OS 3350

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GOULD

An Electrical/Electronics Company

MANUAL PART NO.
80-OS 3350

GOULD OS 3350 40 MHZ
TV MONITOR OSCILLOSCOPE

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Introduction

Section 1

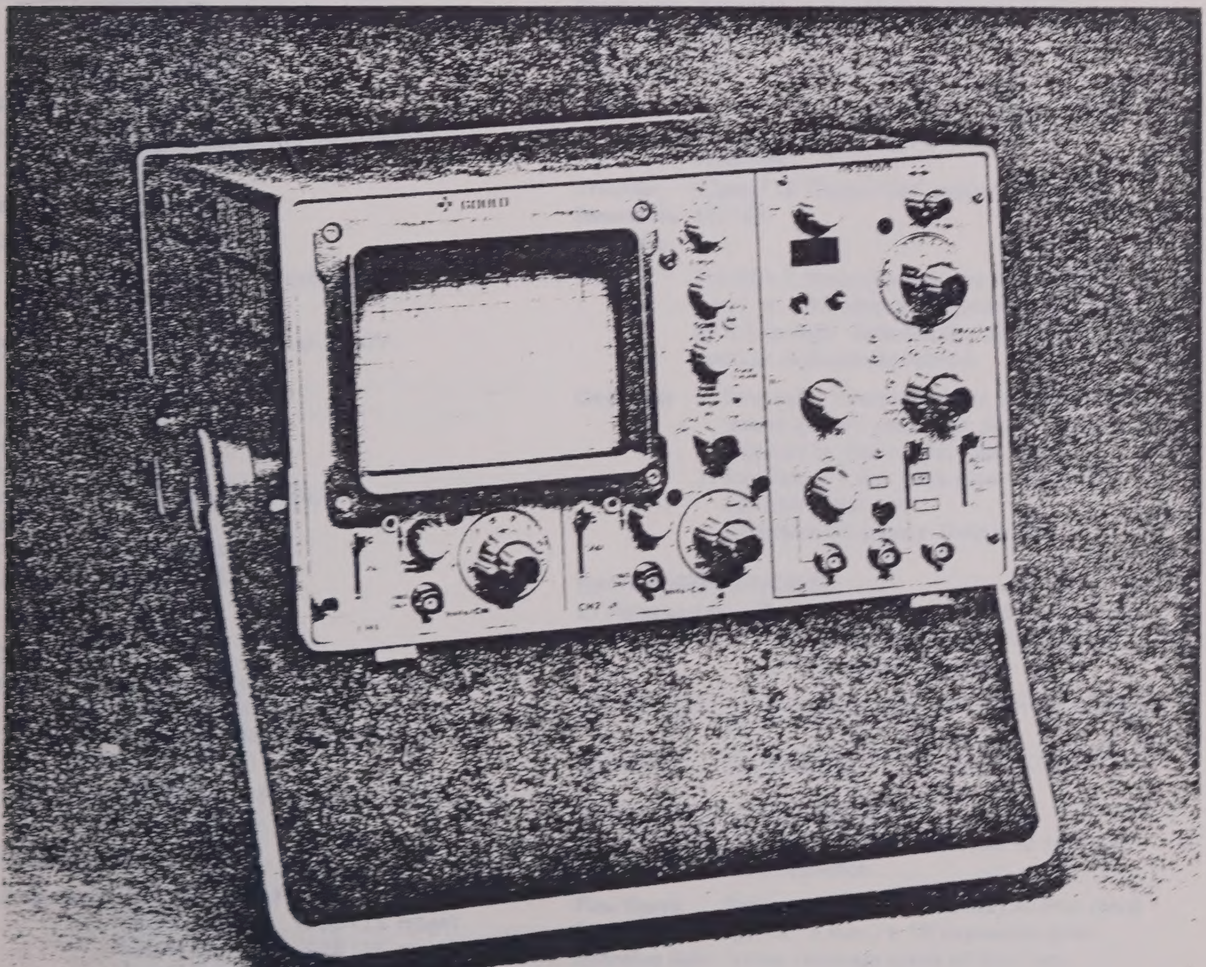
The OS3350/5 oscilloscope provides comprehensive video facilities in addition to normal dual trace single timebase operation.

In its video mode, a black level clamp may be applied to the signal and the timebase may be used to give detailed examination of 525 line television waveforms or to display a picture. It accepts a standard level video signal, and provides the following trigger modes, each of which apply either to Field 1, Field 2 or both fields alternating:- field trigger, line repetitive trigger, L.E.D. identification of any selected line from 001 to 263 and individual lines in the range 15 to 21 inclusive. The triggering may be delayed continuously up to 90µs allowing detailed examination of any part of a line. When displaying a television picture the triggering point selected is indicated by a 'bright-up' on the picture.

To provide maximum brightness on all TV waveforms likely to be encountered, the CRT is operated at an overall voltage of 16kV.

To protect the c.r.t. screen from excessive beam current at low scan rates, an automatic beam current limiting circuit has been included. It should be noted that shading of the c.r.t. display may occur if the trace intensity is increased excessively, whilst operating at slow scan rates. This is not a fault, but simply the correct operation of the beam current limiting circuit. Under such circumstances, reducing the trace intensity to a more convenient viewing level will remove this effect.

When operated as a conventional oscilloscope the timebase retains normal triggering facilities and the Y channels a bandwidth of 40MHz at a maximum intensity of 5mV/div.



Specification

Section 2

DISPLAY

8 x 10cm rectangular faced CRT.
EHT 16kV overall.
External scale 8 x 10cm divisions with centre lines marked in 2mm divisions (illuminated).
Phosphor P31 standard, P7 optional.

VERTICAL DEFLECTION

Normal inputs:-
Two identical input channels which may be operated in chopped or alternate modes, separately or summed.

Bandwidth DC – 40MHz (–3dB) DC coupled, max. amplitude at 40MHz 6 Divisions
2Hz – 40MHz (–3dB) AC coupled, max. amplitude at 40MHz 6 Divisions.
Rise time 9ns.

Input coupling DC-Ground-AC

Sensitivity 5mV/cm to 20V/cm in 1-2-5 sequence with uncalibrated fine gain control giving 2.5:1 reduction in sensitivity. Warning light indicates uncalibrated setting.

Fine shift control facility on CH2.

A x5 facility on CH1 gives maximum sensitivity of 1mV/cm with a bandwidth of DC to 10MHz.

Accuracy ±3% (±5% on x5).

Input Impedance 1MΩ, 28pF

Signal Delay At least 0.5cm visible delay on fastest time-base speed.

Maximum Input Volts (DC plus pk AC) 400V.

OPERATING MODES

CH1 only.
CH2 only.
Channel CH1 and CH2 chopped (500kHz approx.)
CH1 and CH2 alternate.
CH1 + CH2 (Algebraic addition).
NOTE: CH2 may be inverted.

VIDEO INPUTS

Waveform NTSC 525 line video + composite sync with positive-going video, negative-going sync. (Peak white video to sync ratio 100:40 nominal). See Fig. 17.

Video Input Voltage 1V Peak to Peak on centre range of Attenuator.

Input Impedance 75ohms ± 1%.

Input Attenuator Switchable on 3 position level switch.
Upper Position +6dB (2V range)
Centre Position 0dB (1V range)
Lower Position –6dB (0.5V range)

Attenuator Accuracy ±.05dB on +6dB and –6dB positions relative to the 0dB range.

Minimum Video Signal 0.125V p/p when using 0.5V range (12dB below nominal of each input level).

Maximum Video Signal 6V p/p when using 2V range (12dB above nominal level of each range).

Maximum Sustained Input 4V rms.

Maximum Acceptable Noise –30dB with respect to peak luminance amplitude for white noise (0–6MHz) unweighted.

TV DISPLAY FUNCTIONS

Signal transfer via video output to CH2.
Y signal, input set to 50mV/cm dc coupled.

Sensitivity 1 volt peak-peak video input, with video attenuator set to 1V position produces 5 div. ±3%.

Bandwidth Response at 3.58MHz within ±0.08dB of level at 10kHz.

'Clamp Out' Direct through coupling.

'Clamp' Video black level held to 0V ±10mV with no input signal. Hum rejection 20dB minimum.

Transfer Sensitivity Matching 'Clamp' to 'Clamp Out' and/or to Int. Cal. ±0.1dB.

'Picture' Provides Z modulated picture via 525 line raster on CRT, size approximately 8cm wide by 6.5cm high. Selected line and delay position is shown intensified.

Calibrator
1) Internal – interrupts video output and inserts 250mV peak-peak signal ±0.05dB. Selected by front panel push button.
2) External – 1 volt peak-peak output ±1% on front panel pin.
Calibrator frequency 1kHz ±5%.

WAVEFORM RESPONSE

2T Pulse and Bar The pulse amplitude will be within 2% of the bar amplitude for both 'Clamp' and 'Clamp Out' position.

LF Response Tilt on a 50Hz square wave will not exceed 1%.

25μs Bar Tilt on a 25μs will not exceed 1%.

HORIZONTAL DEFLECTION

Sweep Speeds 22 ranges covering 100ns/cm to 1s/cm in 1-2-5 sequence.

Fine Speed Control (Warning light indicates uncalibrated setting) Reduces speed by 2.5 times (slowest speed approx. ½ min.) x 5X expansion gives fastest timebase speed of 20ns/cm.

Accuracy	±3% (±5% on x5).
Trigger Selection	Internal CH1, + or – slope Internal CH2, + or – slope External + or – slope Line + or – slope TV delay or TV (undelayed) Free Run.
Trigger Input coupling	AC, DC, AC LF Rej, AC HF Rej.
Trigger Level Control	a) Manual b) Bright line auto (40Hz to 50MHz).

Trigger sensitivity:

Internal	Manual	– 2mm to 5MHz 1cm at 50MHz
	Auto	– 3mm to 2MHz
External	Manual	– 300mV to 5MHz 1.5V at 50MHz
	Auto	– 500mV at 2MHz

TV TRIGGER

TRIGGER MODES

1. **Line** 15)
16)
17)
18) Line may be selected from field 1 or
19) field 2 or both fields overlaid
20)
21)

2. **Field** Trigger point occurs just after first broad pulse on selected field or both fields overlaid.

3. **Line Repetitive** Trigger occurs before leading edges of syncs on alternate lines. (NB. Field sync information not necessarily required for this mode)

4. **Line Selector** Any of 263 lines may be selected. Line on which trigger occurs shown by LED display. Line number may be advanced or retarded using LINE SELECT switch in 'UP' or 'DOWN' position. Trigger occurs before leading edge of sync pulse.

5. **Field Selector** The field selector switch is used to select either field 1 or field 2 or both fields alternately in any of the available triggering modes (except Line Repetitive).

6. **Trigger Delay** Delays start of sweep from approx. 10μs to 90μs, adjustable by 10 turn control.

7. **Delay Jitter** <10ns.

HORIZONTAL AMPLIFIER

X5 Expansion

Operates on all timebase modes giving fastest sweep speed of 20ns/cm.

Accuracy	±5%.
Beam Finder	Compresses trace to within graticule area for ease of determining the location of an off-screen signal regardless of settings of the vertical and horizontal position controls and within the normal range of the intensity setting.
External X	Sensitivity 1V per cm. 0.2V per cm on X5 expansion. Bandwidth dc-2MHz at 10cms amplitude. Input impedance 100k.

XY OPERATION

CH2 output (rear panel) coupled to Ext X input with X5 X expand.

Bandwidth	dc-1MHz.
Phase Shift	3° at 500kHz. Sensitivity as CH2 input attenuator. Divided by two.
Ext Z mod	(Rear panel.)
Input Impedance	47k
Frequency Response	dc to 10MHz
Sensitivity	1 volt for visible modulation at low intensity +20 volts for blanking from normal intensity.

OUTPUTS

Front Panel Outputs

Calibrator	See "Display Function" section (Sheet 3)
Trigger	Provides a square wave output (approx. 0 to +4V with output impedance approx. 10kΩ). Positive leading edge corresponds to undelayed trigger, trailing edge delayed trigger.
Sync	Provides negative going composite sync of amplitude approx. +5V to 0V with an output impedance of approx. 10kΩ.

REAR PANEL OUTPUTS

1. Normal timebase ramp output via 4mm socket 0 to +10V from <10k.
2. CH2 output via BNC socket, output 100mV per cm deflection.
3. "Picture Output" via 4mm socket (normally linked to 'Z Mod').

SUPPLIES

95-111, 103-121, 111-130V) 45 to 440Hz
190-222, 206-242, 222-260V)
Consumption 70VA approx.

Specification

OPERATING TEMPERATURE RANGE

0–50°C

Full specification is met over range 15°C to 35°C.

SIZE AND WEIGHT

7" (18cm) x $11\frac{3}{8}$" (29cm) x 16½" (42cm).

27 lbs. (12kg.)

ACCESSORIES SUPPLIED

1 off BNC-BNC lead	PL43
1 off BNC-Clips lead	PL44
2 off 4mm plug	PN1244
1 off BNC-BNC lead	PL104
1 off Link (4mm to 4mm)	PL106
1 off Supply lead	[illegible]

OPTIONAL ACCESSORIES

Viewing Hood	[illegible]
Passive Probe Kit	[illegible]
Protective Cover	[illegible]
Trolley	TR4
Timebase Extension lead	PL91
Blank Graticule	[illegible]
Front Panel Cover	[illegible]

3.1 SWITCHING ON

CAUTION: The OS3350 is convection cooled and must always be operated in a position such that air circulation through the bottom and top vents is not restricted.

1. Set the support/carrying handle to the required operating position. The handle is released by pulling outward both fixing bushes when it can then be turned to lock in any one of 5 positions.

2. ENSURE THAT THE SUPPLY VOLTAGE SELECTOR ON THE REAR PANEL IS SET TO SUIT THE VOLTAGE OF THE SUPPLY TO BE USED.
The selector must not be operated while the instrument is switched on. Connect the supply.

WARNING NOTE: The instrument is designed to operate with its frame grounded and for safety it is essential that the ground conductor of the supply lead PL94 is connected to the supply ground.

3. Turn the INTEN control clockwise beyond the POWER OFF setting and ensure that the indicator lamp lights. A trace should be obtainable within 1 min. and full calibrated performance within 15 mins.

3.2 OBTAINING A TRACE

1. To obtain a trace:
   a) Set the MODE switch to CH1.
   b) Set the TRIG SELECT switch to FREE RUN.
   c) Set the DISPLAY to CLAMP or CLAMP OUT.
   d) Operate the TRACE LOCATE push button.
   e) Center the display using the X and CH1 shift controls.
   f) Release the TRACE LOCATE button and set the INTEN control for a display of the required intensity.
   g) Adjust the FOCUS control and ASTIG preset control to obtain a sharply defined trace.

If the TRACE LOCATE button is operated at any other time, the trace should appear. The appearance of the trace toward the top or bottom of the screen can be corrected by the relevant Y shift control unless there is an excessive Y input signal.

Similarly, deflection to either side in the External X modes can be corrected by the X shift control unless due to an excessive X input signal.

If the timebase is in use, the lack of horizontal deflection suggests incorrect triggering.

Once the trace is centered the TRACE LOCATE button should be released and any necessary correction made to the INTEN setting.

3.3 SETTING UP Y CHANNELS

1. Using one of the coaxial input signal leads (PL43 or PL44), or a suitable probe, connect a signal to the CH1 or CH2 input socket.

2. For
   a) Direct coupling of the input signal, set the associated AC, GND, DC input lever switch to DC.
   b) Capacitive coupling of the input signal through an internal 0.1μF capacitor, set the lever switch to AC.

NOTE: When examining low amplitude ac signals superimposed on a high dc level, the lever switch should be set to AC and the sensitivity of the Y amplifier increased as in 4.

3. To locate the baseline, set the lever switch to the GND setting. At this setting, the input signal is open circuit and the input of the amplifier is switched to ground.

4. To adjust the sensitivity
   a) Set the VOLTS/CM switch to a suitable setting. To minimize pick-up at sensitive settings, it is essential to ensure that the ground lead connection is near to the signal point.
   b) If necessary, adjust the concentric VARIABLE control.

NOTE: The range of the VARIABLE control is uncalibrated. A warning UNCAL light mounted adjacent to the VARIABLE control is lit, once out of the CALIBRATED position.

At the CALIBRATED setting, the calibration corresponds to the setting of the VOLTS/CM switch.

5. For vertical movement of the trace, adjust the Y shift controls (identified with vertical arrows).

6. If, under no signal conditions, trace movement is detected when the VARIABLE is altered, reset the BAL preset control. If there is subsequent movement when the VOLTS/CM control is switched between ranges, the STEP BAL preset control should be adjusted. Access to this control is through the bottom cover.

7. Preset gain adjustment for each channel is available with access to the control through the bottom cover. This should be set for 5cm of deflection on the 200mV/cm range with the input coupled directly to the 1V calibrator output.

NOTE: These preset controls will only need adjusting at infrequent intervals or after a large change of ambient temperature. They should not be adjusted within 15 mins. of switch on. Check that the input coupling switch is set to GND.

3.4 SINGLE TRACE OPERATION

1. For single trace operation on the CH1 channel, set
   a) The MODE switch to CH1.
   b) The CH1 shift control (indicated by double ended vertical arrow) to mid setting.
2. For single trace operation on the CH2 channel set
   a) The MODE switch to CH2.
   b) The CH2 shift control (indicated by double ended vertical arrow) to mid setting.

3. High sensitivity operation with a bandwidth of dc to 10MHz can be obtained on CH1 by pulling the SHIFT control which increases the sensitivity 5 times, i.e.

1mV/cm with the sensitivity set to 5mV/cm

2mV/cm with the sensitivity set to 10mV/cm

4mV/cm with the sensitivity set to 20mV/cm

Beyond this it is better to revert to normal operation.

4. It is possible to obtain useful higher sensitivities with unspecified overall performance by cascading the two channels. The input signal should be coupled into CH2.

OUTPUT socket on the rear panel coupled to the CH1 input using a coaxial connector, PL43.

The MODE switch should be set to CH1. The CH2 output provides 0.1V/cm of normal CH2 display, i.e. an additional gain of x10. DC offsets and drift will necessitate the use of ac coupling in this mode and amplifier noise will negate the use of the full sensitivity of 100μV/cm.

NOTE: That for ease of operation for video measurements, a dual action shift control is provided on CH2 to give fine and course control.

3.5 DUAL TRACE OPERATION

In the dual trace condition, the beam switching function is in operation and results in the independent display of two signals simultaneously. Two modes of beam switching – chopped or alternate – are used, selected by the setting of the MODE switch. At any fast setting from 0.1μs/cm to 0.5ms/cm inclusive, the alternate mode is recommended. At slow settings from 1ms/cm to 1s/cm, inclusive, and EXT X, the chopped mode is preferable. For EXT X the chopped mode is essential to give two trace operation.

1. For dual trace operation, set
   a) The CH1 shift control to mid position.
   b) The CH2 shift control to mid position.
   c) Select ALT or CHOP or MODE switch.

3.6 TIMEBASE OPERATION

The speed of the timebase is determined by the setting of the TIME/CM switch. In addition to selection of the speed of the internal timebase, the switch has a functional setting, EXT X in which the internal timebase is inoperative. The gain of the internal X amplifier may be increased by 5 times by pulling out the PULL X5 control on the inner shift control. This facility is available at all settings including EXT X. The facility effectively increases the sweep length from 10cm to 50cm and thus allows close examination of any portion of the trace. Any portion of the increased sweep length may be selected for viewing on the display by adjusting the X shift controls (identified by horizontal arrows). The fine shift control will move the display by approximately 1cm when the PULL X5 is not operative and by 5cm in the magnified mode.

A particular advantage of this facility is to increase the maximum sweep speed to 20ns/cm.

1. To adjust the timescale of the horizontal axis
   a) Set the TIME/CM switch to the required setting.
   b) If necessary, adjust the concentric VARIABLE.

NOTE: The range of the VARIABLE control is approximately 3:1. The VARIABLE control is uncalibrated and a warning light, adjacent to the VARIABLE control, lights in the UNCAL position. At the CALIBRATED setting only, the calibration corresponds to the setting of the TIME/CM switch.
Selection of the 1sec/cm range and full use of the variable control, provides a total sweep time of approximately 0.5 min.

3.7 TRIGGER

The timebase may be operated in a FREE RUN condition or more normally, triggered from the positive or negative slope of a signal as determined by the setting of the TRIGGER SELECT switch. The triggering sources selected by the TRIG SELECT switch are as follows:-

a) The mains supply line input frequency derived internally from the supply transformer.

b) CH1 or CH2 amplifiers (irrespective of which beam is displayed).

c) Internally generated signals from the VIDEO input. (See section 3.8)

d) Any external triggering source connected to the EXT TRIG socket.

The LEVEL control concentric with the TRIG SELECT switch allows selection of the triggering point on the trigger waveform and hence determination of the start of the horizontal trace. When the LEVEL control is set to AUTO, the trigger circuit automatically biases itself to a sensitive trigger level condition. In the absence of a trigger signal in this mode, the timebase will free run and maintain a displayed sweep at the selected speed. The TRIG SELECT switch is used in conjunction with the TRIGGER COUPLING lever switch. This switch connects different networks into the trigger amplifier circuit and is effective on all settings of the TRIG SELECT switch. However, for TV trigger operation the coupling switch should be set to AC or DC(TV).

The operating facilities available at the 4 settings of the lever switch are as follows:-

1. AC. This is a wideband trigger mode used for the most common triggering signals.

2. AC LF REJECT. A filter is switched into circuit to reject low frequencies. High frequency triggering may be effected from low level waveforms with applicable high ripple content.

3. AC HF REJECT. A filter is switched into circuit to reject high frequencies. Low frequency triggering may be effected from complex waveforms containing high frequency components.

4. DC TV. A wideband trigger mode, which is most useful at very low frequencies. The Y-input coupling must also be DC for this mode to be effective on internal trigger. It is also used for triggering the instrument on television.

To operate the instrument in its standard mode (i.e. on Non-TV waveforms) triggering is effected as follows:-

1. Set the TRIG SELECT switch to the required trigger signal (i.e. MAINS LOCK, CH1, CH2 or EXT).

2. Set the DISPLAY switch to either 'CLAMPED' or 'UNCLAMPED'.

3. Set the TRIGGER COUPLING switch to the required setting.

4. On most waveforms it is convenient to select AUTO. If this is not required, adjust the LEVEL control so that the trace starts at the required point on the waveform. If the timebase is not required to be triggered, set the TRIG SELECT switch to FREE RUN.

NOTE: If, in the Auto mode, the frequency of the trigger is less than approx. 40Hz, or the amplitude is too low for reliable triggering, the timebase automatically changes to a free run condition. This condition produces a trace at the selected sweep speed.

3.8 TIMEBASE OPERATION IN TV MODE

The timebase is designed to operate from positive-going video (negative sync) of 1V peak to peak amplitude. Into the VIDEO I/P socket.

The timebase will allow two types of display of video information:-

a) PICTURE, where a complete 625 line raster is displayed on the screen, covering approximately 6.5cms x 8cms.

b) CLAMPED or UNCLAMPED, where the video waveform producing a line or lines of information may be examined.

For the latter condition, the timebase functions in the normal manner but receives its trigger information from an internal sync separator system.

For the PICTURE requirement the timebase is switched out automatically, and line and field timebases are introduced to generate the required raster.

3.9 OPERATION IN THE 'CLAMP' OR 'CLAMP OUT' MODES

Video waveforms connected to the VIDEO INPUT sockets may be examined in these modes after the VIDEO OUTPUT SOCKET is coupled to either the CH1 or CH2 Y input socket and that channel selected for display.

In the CLAMP mode, the video information is locked to Black Level for 0V dc on the Y display. An incoming 1V peak to peak video signal (Peak White to sync tips) viewed on the CRT should display a 5cm amplitude with the video attenuator set to 0dB and the Y attenuator switch at DC, 50mV/cm. Because of the action of the clamp, changing picture content does not affect the position of the mean dc level on the Y-display. This makes this mode particularly suitable for viewing waveforms where substantial picture level changes or LF ripple may exist.

The 'CLAMP OUT' function does not have this facility, this mode being particularly suitable to the inspection of video waveforms where changes in APL (Average Picture Level) are minimal or where higher accuracy is required on the waveform display.

Setting up for these functions is accomplished by the following procedure.

1. Connect a lead (e.g. PL104) between the VIDEO OUT socket on the timebase front panel and the Y CH2 input, then set the mode switch for CH2 display.
(CH1 may be used as an alternative if required.)
2. Switch to 'CLAMP' or 'CLAMP OUT' mode as required.
3. Set the Y CH2 input to GROUND and the attenuator range to 50mV/cm.
4. Set the TRIGGER SELECT switch to FREE RUN and centre the Y CH2 trace using the multiturn Y-shift control.
5. Set the VIDEO LEVEL lever switch to the desired signal amplitude (i.e. 1V ±6dB) and insert the video signal.
6. Set the TRIG SELECT switch to TV or OVERLAY according to whether a delayed sweep is required or a delayed sweep superimposed on the undelayed waveform.
7. Set the TRIGGER COUPLING switch to DC TV or AC.
8. It is preferable to begin by setting the timebase range switch to 10μs/cm so that the display will show about 1½ lines of information.
9. Select the required line or field to be viewed, using the LINE SELECT switch (see section 3.11).
10. Now adjust the trigger level control until a stable trigger on the required line is obtained. This position is approximately central on the control. (The trigger level allows about 90° of angular rotation over which the control may be set for this requirement.)

3.10 DELAY CONTROL

When the TV is selected on the TRIGGER SELECT switch the DELAY CONTROL can be varied to give up to about 90µs of delay from the trigger point.

In the TV OVERLAY position, the delayed signal is displayed, superimposed on the nondelayed signal. The trigger point for the non delayed signal is just before the Line sync pulse preceding the required Line.

NOTE: If the DELAY control is not operative, it may be necessary to re-adjust the Trigger Level control.

3.11 LINE SELECTION

The operator may view if required 7 pre-selected video lines in the range 15–21 by direct access on the switch.

LINE REPETITIVE triggering is a useful function where pulse and bar generators are to be used. In this mode, the sync waveform does not need to contain field pulse information. Triggering is performed on every alternate line. The DELAY control may be used here for analysis of relative pulse heights etc. using the graticule markings.

On LINE SELECTOR position, an LED display will illuminate, showing the Line number on which the timebase is triggering. This may be set to any integer between 1 and 263. The selected number is increased with the Line select switch in the 'UP' position and decreased with the switch in the 'DOWN' position. The display will step slowly for 4 counts and the speed up.

3.12 FIELD SELECTION

In any of the TV trigger modes except Line Repetitive, the operator has the choice of which field he wants to view. With the FIELD SELECT switch in the F1 position the trigger point is at the Line selected in field 1. In the F2 position, it is in field 2. In the BOTH position, the trigger point is alternately in field 1 and field 2, at the Line selected. Note that Line 263 field 2 is the same as Line 1, field 1.

3.13 PICTURE DISPLAY

A visual display of the 525 line raster is available when the display switch is set to 'PICTURE'. The raster occupies an area approximately 6.5 x 8cm on the screen.

NOTE: That the full signal content is displayed and with the standard video pattern the first vertical ½cm displays test signals and Teletext information prior to the start of the picture.

The video information for modulating the CRT is supplied from the 'PICTURE DRIVE' socket on the rear of the instrument, and is linked to the Z mod socket. The PICTURE DRIVE information contains all the blanking pulses required during flyback, but a short field blanking period is used to enable the operator to observe Test signals etc. preceding the picture content.

An additional bright-up is applied to the picture which starts approx. 1cm from the end of the previous line and extends along the selected line for the period defined by the DELAY control. This is used as a pointer to the selected line or lines. The end of the "pointer" indicates the setting of the DELAY control. On FIELD trigger, this pointer over-rides the flyback blanking. If this feature is not required when viewing a picture, the DELAY should be set to minimum.

The 'PICTURE' mode may be displayed by the following procedure:

1. Connect a lead (PL104) between the 'VIDEO OUT' socket on the timebase and the Y CH2 input, and set the mode switch for CH2 display.
2. Set the Y sensitivity to 50mV/cm and the input to DC.
3. Connect the link (PL106) between the PICTURE DRIVE and Z mod sockets on the rear panel.
4. Set the VIDEO ATTENUATOR lever switch to the desired video input level and insert the video signal.
5. Set the DISPLAY switch to 'PICTURE', adjust the Y shift for a central raster and the Intensity control for the best display.

NOTE: It is not necessary to trigger the timebase for this display mode, however, it is useful to have the instrument set up as in Section 3.9 in order that picture waveforms can be analysed immediately on switching away from the PICTURE position. The 5 x expansion is still available for PICTURE display.

3.14 EXTERNAL X

In this condition, the external signal is applied directly to the Internal X amplifier to produce a calibrated (1V/cm) horizontal deflection via the EXT X socket at the rear of the instrument. Dual trace Y operation is only available if chop is selected. The bandwidth is 2MHz.

1. Set the 'TIME/CM' switch to EXT X.
2. Set the display switch to 'CLAMP' or 'CLAMP OUT'.
3. Connect the signal to the EXT X socket.

3.15 X-Y MODE

It is possible to use the flexibility of the two Y inputs for X-Y displays.

1. Set the TIME/CM switch to EXT X.
2. Set the CH2 input switch to DC or AC as required.
3. Connect the external signal which is to be used for the X deflection to the CH2 socket.
4. Select x5 amplifier gain.
5. Couple 'CH2 OUT' (rear panel) to EXT X input with a coaxial lead, PL43.
6. Set the display switch to 'CLAMP' or 'CLAMP OUT'.

7. Operate the CH1 channel as for single trace operation and use the CH2 VOLTS/CM switch to control the X deflection. The CH2 shift is inoperative but note that the X deflection is 2 times less sensitive than that indicated by the CH2 VOLTS/CM switch.

3.16 ADDITIONAL FACILITIES

Use of optional Passive Probe

A x10 passive probe may be used to extend the voltage range and increase the input impedance of the Y amplifiers. The input resistance of a Y channel is 1MΩ shunted by approximately 28pF. The effective capacity of the input lead must be added to this, and the resultant impedance will sometimes load the signal source. Therefore it is advisable to use a 10MΩ x 10 probe. This reduces the input capacity and increases the input resistance at the expense of the sensitivity. The probe contains a shunt RC network in series with the input, and forms an attenuator with the input RC of the Y channel. To obtain a flat frequency response it is necessary to adjust the capacitance of the probe to match the input capacity of the Y channel as follows:

1. Set the timebase display switch to 'CLAMP' or 'CLAMP OUT'.
2. Set the TIME/CM switch to 0.2ms/cm.
3. Set the Y channel VOLTS/CM switch to 20mV/cm.
4. Set the trigger to AUTO and the source to CH1 or CH2 according to which channel the probe is to be set up on.
5. Connect the probe to the CAL 1V pin protruding from the timebase front panel.
6. Set the adjustable capacitor in the probe tip or termination with a small trimming tool for a level response with no undershoot or overshoot visible on the display.

Cal 1V Output and Internal Cal Signal

The 1V output pin provides a DC coupled positive-going square wave signal of 1V + 1% at 1kHz approx. for calibration checks. The source impedance (1 volt) is 1kΩ, with a signal rise time of approx. 100ns.

When the instrument is to be used with TV signals in the 'CLAMP' or 'CLAMP OUT' mode, the calibrator may be used to provide an internal reference signal when the CAL button is pushed. This automatically interrupts the out-going video signal to the Y channel. The CAL signal is 250mV ±0.5dB at approx. 1kHz. This will provide a 5cm display when the Y input is set at 50mV/Div. Triggering on this signal should be done by switching the TRIG SELECT switch to CH2 (or CH1 if this channel is used for the TV display).

Z Mod

This socket on the rear panel in addition to providing a link for the picture modulation also allows DC coupled signals to be applied to the tube.

The CRT trace is intensified by a negative input, and blanked by a positive input. The required amplitudes are:-

a) 2 volts for visible intensity modulation.

b) +20 volts for blanking at normal intensity.

This facility is available in any operating mode of the instrument except PICTURE.

Ramp

This socket on the rear panel provides a dc coupled positive-going timing ramp or approximately 10V amplitude, generated by the timebase. The source impedance is 4.7kΩ and the ramp may be used for instance as a drive for external frequency swept oscillators to allow a display of voltage against frequency.

3.17 PULSE MEASUREMENT TECHNIQUES

One use of the OS3350 is to measure small amounts of distortion on test waveforms such as sine squared pulse and bar signals. A useful measurement technique for such applications is to use the second input channel to provide a reference line or pair of lines on the screen avoiding parallax errors of comparison against a graticule. The following description of a method of measuring droop of a pulse top can be modified as necessary to measure pulse overshoot, etc.

With the video signal coupled to the CH2 input and the timebase triggered as necessary to view the full width of the pulse top, select dual channel operation as ALT (or at low repetition rates CHOP). If the CH1 input coupling is set to GND, a single horizontal line is superimposed on the pulse. Adjust the CH1 shift control to position this reference trace on the left hand end on highest point of the pulse top to be measured. It is now easy to detect on the pulse top small variations from the reference line and to measure the deviation against the graticule.

An extension of this technique provides two reference lines for more accurate assessments of small deviations. Connect the CH1 input directly or via a probe to the CAL output pin of the OS3350. If a probe is used first check that it is correctly compensated (see Section 3.16). Set the CH1 input coupling to DC. As this calibration signal is not synchronized to the video input signal used for trigger, its square wave shape will appear as two parallel lines. Operate the CH1 VOLTS/CM, VARIABLE sensitivity and shift control to position these two lines to correspond to the maximum and minimum points of the pulse top under observation. Without altering the position of the VARIABLE control, increase the CH1 sensitivity by 3 switch positions to increase the spacing of the reference lines by 10 times. Operate the CH1 shift control to align one of the lines with a graticule line and measure their spacing against the graticule. The peak to peak pulse aberration (the original spacing of the reference lines) is then one tenth of the final measured spacing which can be expressed as a percentage of pulse height of the original pulse height if required.

It should be realized that actual voltage measurements of pk to pk aberration are calculated with respect to the CH2 sensitivity and the actual setting of CH1 sensitivity is irrelevant to the measurement.

To improve discrimination of pulse aberration measurements, it is possible to overscan the 8cm vertical scale by about 50% without introducing significant distortion to a conventional sine squared pulse and bar.

A further variation to this technique of using the second channel as a reference is to drive it from any other square wave source but via a stepped attenuator, allowing the reference lines to be incremented in steps of dB's or parts of dB's.

The OVERLAY facility can be used for measurement of the relative heights of Pulse and Bar on a standard pulse and bar test waveform. This gives an idea of the Luminance to chrominance ratio, and an indication of the overall frequency response of the channel. The line with pulse and bar waveforms on it is selected with the VIDEO SELECT switch, the TRIGGER SELECT switch is set to OVERLAY and the timebase is set to a suitable range (e.g. 10 s/cm). Two superimposed traces should be visible, one being a delayed version of the other. By varying the DELAY CONTROL, the pulse can be brought to coincide with the centre of the bar. The relative heights can then be measured as described above.

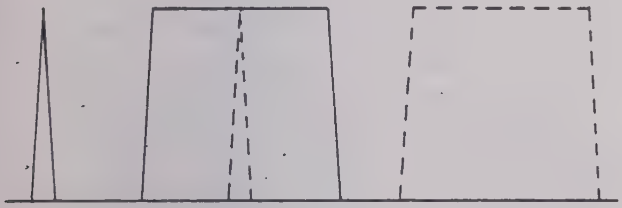


Diagram showing OVERLAY mode to display pulse and bar waveform.

Circuit Description

Section 4

For convenience, the circuit reference of any component can be used to determine its location in the instrument.

1 – 99	Frame or interconnection.
100 – 199	CH1 and CH2 pre-amplifiers and attenuators.
200 – 299	Beam switch and delay line drive amplifier.
300 – 399	Delay equaliser and Y O/P amplifier.
400 – 499 500 – 599	Timebase
600 – 699 700 – 799	TV Circuitry
800 – 899	Power supply and EHT supply.
900 – 999	Bright-up amplifier and X output amplifier.
e.g. R374	is part of the Y output amplifier.
D801	is part of the EHT oscillator.

The circuit diagrams are generally arranged for each printed board assembly or group of boards. These diagrams include some of the switches, potentiometers, etc., closely associated with the circuit although these components may be mounted on the frame. Consequently not all such components appear on the interconnection diagram, Fig. 9, and where it makes the circuits easier to follow, some components appear on more than one circuit.

In addition to the relevant circuit diagrams, useful reference can be made to the waveform diagram, Figs. 10 and 11, when following the description of the timebase section.

4.1 THE BLOCK DIAGRAM

The block diagram for the complete instrument is shown in Fig. 1. It is not intended to be a full logic diagram but details the functional points of the circuit and their interrelation. The circuit can readily be divided into two main sections which are the Y and the X deflection circuits. The latter includes the timebase with the associated trigger system and the video signal and synch separator system. The bright-up or Z modulation function is described as part of the timebase function.

The main X and Y signal paths for a dual trace display using the main time sweep only, are indicated by the heavy lines.

Y CHANNELS

The switch attenuator, pre-amplifier and trigger amplifiers are identical for the two Y channels. CH1 differs in having invert and output facilities. The state of the decade steps of attenuation and 1, 2, 5 sequence of pre-amp gain switching are determined by the sensitivity selected.

The use of the x5 GAIN on CH1 increases its basic sensitivity to 1mV per centimeter but reduces the overall bandwidth to 10MHz.

The channel switch is a fast electronic switch with the equivalent of a change-over action as shown. It selects either the CH1 or the CH2 signal to be passed to the subsequent stages and is controlled from a bistable. In the chop mode the bistable is driven by continuous pulses from the free running multivibrator, switching the beam between the CH1 and CH2 signals as the X sweep progresses. In the alternate mode, the multivibrator acts as a monostable generating a single pulse to reverse the beam switch at the end of each timebase sweep, giving alternate CH1 and CH2 sweeps. In the ADD mode, both the CH1 and CH2 switches are closed and the two signals are summed algebraically. On CH1 and CH2 only the appropriate switch is closed allowing that signal to pass.

The signal from the selected channel is passed via a delay line and amplifiers to the Y deflection plates of the CRT. This delay allows examination of that point in the waveform which initiated the sweep because the deflecting signal reaches the Y plates after the time sweep has been initiated and the trace brightened.

THE EXTERNAL X I/P

When external X is selected, the trace is brightened and the timebases are inhibited. The amplified X input signal passes through the X gate to the main amplifier.

THE TIMEBASE

The purpose of the timebase system is to generate a linear ramp to deflect the spot in the X direction. The trigger system initiates each sweep from the incoming or other signals, normally to obtain a stationary display of a repeated waveform.

The internal or external signal as selected is amplified by the trigger amplifier to drive a trigger circuit. If the timebase is ready to commence a sweep, a transition of the trigger circuit will set the timebase bistable which in turn initiates the ramp. This signal is passed through the X gate and X output amplifier to the X deflection plates of the CRT. At the end of the sweep, when the ramp reaches the required level the bistable is reset, returning the ramp to its original level. During the period of sweep the trigger gate is prevented from passing trigger pulses to the bistable and this inhibition is maintained by the hold-off circuit until the ramp generator is fully recovered, ready for the next sweep to commence on the next trigger pulse, when the cycle repeats.

The bright-up amplifier normally holds the CRT beam in the cut-off state. The output of the bistable which allows the ramp to operate, also feeds the bright-up amplifier to raise the intensity of the CRT spot to the level determined by the intensity control.

At the end of sweep this output of the bistable is reset and blanks the trace during the flyback period. If the Y channels are being switched in the chopped mode, the differentiated output of this multivibrator is also fed to the bright-up amplifier to blank the trace while the Y switching transition takes place. This leaves the appearance of two separate traces for CH1 and CH2 on the screen unless the sweep speed is higher than that normally required for chop operation.

TIMEBASE TRIGGER MODES

The trigger signal for the timebase selected from internal, external, TV or mains power supply frequency sources, is ac. or dc. coupled before being fed into the trigger

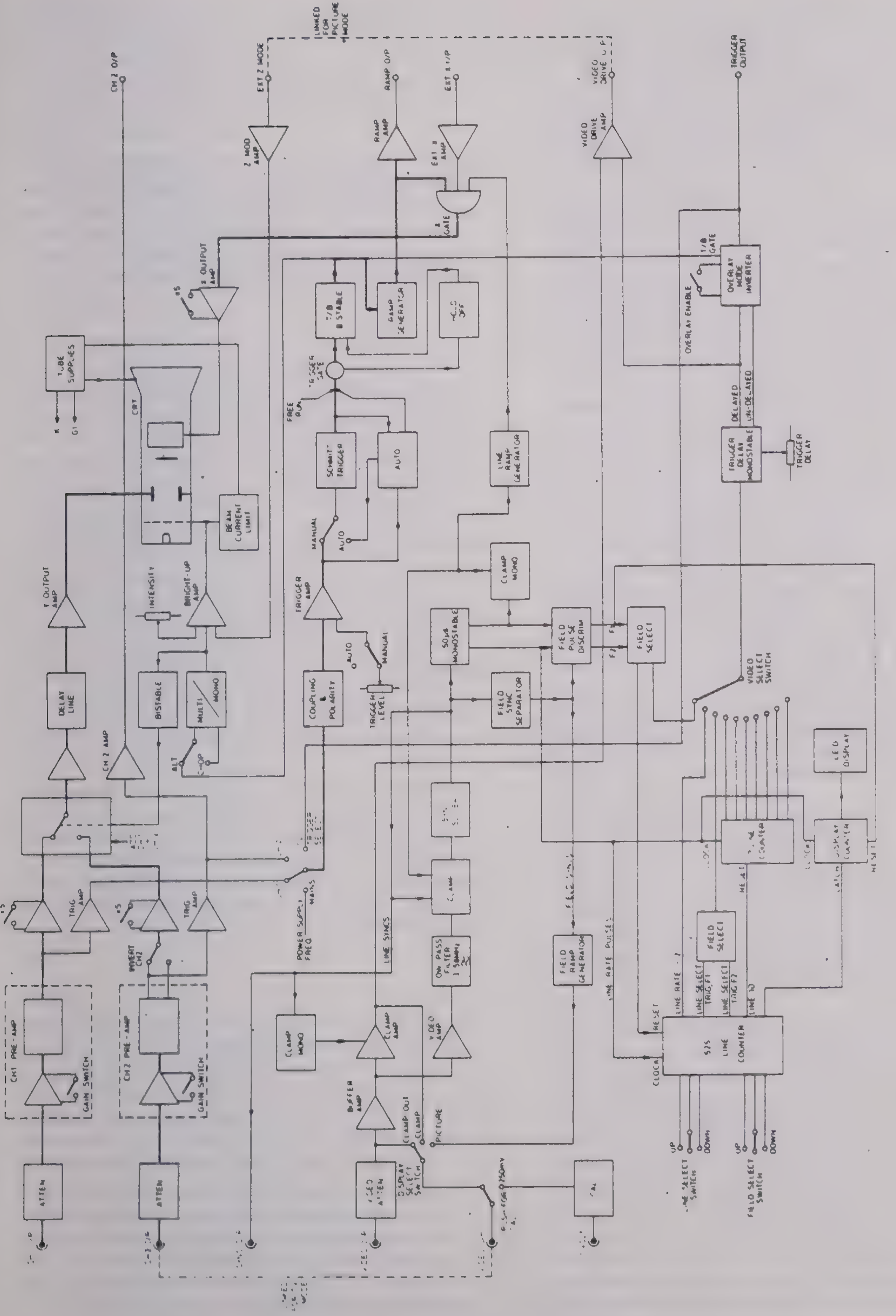

CH 2 O/P
EXT Z MODE
LINKED FOR PICTURE MODE
RAMP O/P
EXT X I/P
VIDEO DRIVE O/P
TRIGGER OUTPUT
Z MOD AMP
RAMP AMP
EXT X AMP
VIDEO DRIVE AMP
X GATE
X OUTPUT AMP
x5
T/B BISTABLE
RAMP GENERATOR
HOLD OFF
T/B GATE
OVERLAY MODE INVERTER
OVERLAY ENABLE
TUBE SUPPLIES
K
G1
CRT
TRIGGER GATE
FREE RUN
SCHMITT TRIGGER
AUTO
LINE RAMP GENERATOR
DELAYED
UN-DELAYED
TRIGGER DELAY MONOSTABLE
TRIGGER DELAY
BEAM CURRENT LIMIT
Y OUTPUT AMP
INTENSITY
BRIGHT-UP AMP
MANUAL
AUTO
TRIGGER AMP
CLAMP MONO
50/4 MONOSTABLE
FIELD PULSE DISCRIM
F1
F2
FIELD SELECT
VIDEO SELECT SWITCH
AUTO
MANUAL
TRIGGER LEVEL
COUPLING & POLARITY
FIELD SYNC SEPARATOR
DELAY LINE
BISTABLE
MULTI MONO
ALT
CH 2 AMP
LED DISPLAY
TRIG AMP
x5
TRIG AMP
INVERT CH2
CH1 PRE-AMP
GAIN SWITCH
CH2 PRE-AMP
GAIN SWITCH
ATTEN
ATTEN
LINE SYNCS
POWER SUPPLY FREQ
MAINS
LOW PASS FILTER
CLAMP
CLAMP MONO
CLAMP AMP
VIDEO AMP
BUFFER AMP
CLAMP OUT
CLAMP
PICTURE
DISPLAY SELECT SWITCH
VIDEO ATTEN
CAL
FIELD RAMP GENERATOR
LINE RATE PULSES
FIELD SELECT
RESET
CLOCK
525 LINE COUNTER
LINE RATE
LINE SELECT TRIG F1
LINE SELECT TRIG F2
LINE 10
LATCH
RESET
DISPLAY COUNTER
UP
DOWN
LINE SELECT SWITCH
UP
DOWN
FIELD SELECT SWITCH

FIGURE 1 BLOCK DIAGRAM

amplifier. This is biased by the required trigger level and the resultant output passed to the trigger circuit where the waveform is squared up.

In the FREE RUN mode the trigger gate is permanently energized, and the timebase bistable is set again at the end of each hold-off period.

When AUTO coupling is selected, the trigger amplifier is automatically biased to the optimum working point for sensitive operation of the trigger. If the signal level out of the trigger amplifier is insufficient to operate the trigger circuit, a further output from the auto circuit causes the timebase to free run, displaying the necessary bright line trace.

TV OPERATION

In all TV modes of operation, the oscilloscope is driven from the signal applied to the VIDEO INPUT socket. This signal is fed to a 75Ω attenuator which introduces 6 or 12dB of attenuation. 6dB is normally in circuit allowing the attenuator switch to select ranges +6dB or −6dB from nominal. In the CLAMP-OUT mode, the output from this attenuator is switched directly to the VIDEO OUTPUT socket which is coupled externally to the CH2 input socket for display against the timebase.

The output from the attenuator is fed also through a buffer amplifier to a Black level clamp amplifier and the output from this is selected as the VIDEO OUTPUT when the Display Select switch is set to the CLAMP mode. The level clamped signal also drives a comprehensive sync separator system which is described in detail later. When the PICTURE mode is selected the VIDEO OUTPUT signal is derived from the Field Ramp Generator.

To complete the necessary raster, the sync separator circuit drives a Line Ramp Generator. The output of this is switched into the X deflection amplifier in place of the normal timebase sweep signal by the X Gate. The clamped video signal, buffered through video drive amplifier has to be linked externally from the PIC. DRIVE to the adjacent EXT Z MOD input to complete the picture display.

DELAY

When either of the TV modes is selected by the Trigger Source switch, the timebase is triggered from the sync separator system via a delay monostable. In the TV position the trigger polarity is such that the sweep is triggered from the trailing edge, introducing the delay as determined by the monostable period and set by the delay control. This has a single range of approx 90μs.

In the OVERLAY position the polarity of the output of the monostable is alternately inverted after every timebase sweep, so that the timebase can trigger twice during the line period, once just before the line sync., and once after the delay set on the DELAY control, so that a delayed and an undelayed trace appear superimposed on the screen.

In the PICTURE mode, an additional bright-up signal is applied to the Z modulating signal during the delay period and this is used to identify a line or lines selected by the TV trigger system. The length of this bright-up line indicates the delay period pointing to that section of the video waveform which will be displayed against the timebase on switching from PICTURE to the CLAMP or CLAMP-OUT modes of display.

SYNC SEPARATION

A portion of the video signal is taken off the video attenuator output and amplified by about 5 times. The high frequency components of this signal (above 3.5MHz) are removed by a low pass filter, i.e. the Chroma and sound signals. The filtered signal then passes to the line sync separator. This stage consists of two circuits; a primary sync separator which sets up the initial conditions, and a secondary sync separator in a regenerative loop with a clamp monostable multivibrator to provide a hard lock.

The primary sync separator provides sync pulses to operate an internal black level clamp operating during the back porch period of the video waveform, so dc. restoring the signal. The secondary sync separator receives the clamped video and feeds sync pulses to a 50μs monostable multivibrator. Since this circuit has a time period exceeding the half line periods (32μs) during the Field sync period, only the full line sync pulses at 64μs intervals are allowed to pass through it. The undelayed leading edge from the monostable (coincident with the leading edge of the line sync pulse) is fed to the clamp monostable. This has a period of 5μs and provides a delay just exceeding the line sync pulse period (4.7μs). A second clamp operating during the back porch period is actuated by the delayed edges from the output pulses of this monostable, thus providing the regenerative lock action with the secondary sync separator.

Field sync separation from Composite Sync information is achieved by a single transistor amplifier with RC coupling at both its input and output. The time constant of the input circuit to the stage is chosen such that it only responds to the broad Field Sync pulses which cause a change of mean dc. level. The output RC network operates in such a way as to only select the narrow 4.7μs gap occurring between the first and second broad Field sync pulses.

Even Field (F1) and Odd Field (F2) pulses are separated by gating the detected field pulse with the two outputs from the 50μs monostable. The First Even Field Broad pulse begins in phase with the position normally associated with the leading edges of the line sync pulses, whereas the Odd Field pulses begin half a line period late. Since the gap between the first and second broad pulses occurs 27.1μs after the leading edge of the first Broad pulse, then the Even detected field pulse occurs within the 50μs time period of the monostable.

The Odd field detected pulse, however, occurs 58.9μs after the phase position of the line sync pulses, and therefore outside the time period of the monostable. By comparing inverted and non-inverted outputs from the mono-

stable with the detected field pulse, then F1 and F2 pulses can be discriminated. Outputs from the Line and Field pulse separators are then used to drive the Line and Field ramp generator circuits used for the PICTURE mode.

LINE COUNTER SYSTEM

The 50μs monostable which provides a regular pulse train in phase with the leading edges of line syncs is used to drive the Line counter. The delayed edge of the monostable is used to clock the counter; and hence clocking occurs after about ¾ of the line period has occurred. The 525 line counter consists of a 12 bit binary counter which for all modes except when the line selector display is required, is reset by the field sync pulse: F1, F2 or both depending on position of FIELD SELECT switch. When the line selector display is to be used by selecting the appropriate position on the VIDEO SELECT switch then internal gating is arranged for the counter to make it count to 263 independently of the position of the incoming field sync pulses.

VIDEO SELECT SWITCH POSITIONS

1. FIELD TRIGGERING

This switch position selects either the F1 or the F2 output from the field pulse discriminator, or both added together, depending on the position of the FIELD SELECTOR switch. These outputs are then used to trigger the DELAY monostable.

Since the detected field pulse occurs in the gap between the first and second broad pulses, then information prior to this, within the field period (e.g. the first set of equalizing pulses) cannot be displayed in this switch position. Therefore, for such requirements the Line selector display position should be used.

2. LINE REPETITIVE TRIGGERING

This position is useful for displaying waveforms from Pulse and Bar generators which produce repetitive line-by-line picture information. The first bit (Q1) output for the counter is used to trigger the DELAY monostable on this switch setting. This provides the monostable with triggering on alternate lines, thus preventing an overlap problem when the monostable DELAY period is extended to maximum. Note that the 525 line counter is normally reset by the F1 or F2 Field sync pulse, however, some pulse and bar generators do not produce Field information, and the system will operate satisfactorily without such reset.

3. LINE SELECTOR & DISPLAY

The line selector is useful in that any of 263 lines in either field may be individually selected (Line 263 of field 2 is the same as line 1 of field 1), with a numerical counter displaying the number of the selected line.

In this mode the 525 line counter provides its own reset signal when the 525 count is complete. The position of the reset pulse with respect to that of the F1 sync pulse is random although constant as long as the counter maintains its 525 count. By pressing the LINE SELECT switch for UP or DOWN the counter is made to count to either 526 or 524 respectively, for a short period, thus altering the position of the counter reset pulse with respect to the F1 pulse. A completely independent counter, which drives the LED display is clocked by the same line rate pulses which drive the 525 line counter, and is latched when the 525 line counter resets. The display counter, which is reset by the F1 field pulse, then counts the number of line rate pulses which have elapsed between the F1 pulse and the 525 line counter reset, and indicates the count on the LED display.

If field 1 is selected, the DELAY monostable is triggered when the 525 line counter reaches 521. Because the counters are clocked 50μs after the leading edge of the line syncs, timebase trigger will occur about 10μs before the next line pulse occurs. A count of 521 is needed because line 1 occurs 3 lines before the F1 pulse.

If field 2 is selected, the DELAY monostable is triggered after 259 counts, in other words 262 line periods before the equivalent line in field 1.

The display counter never indicates a number greater than 263. This is because the 525 line counter is made to always reset during the field 1 period (i.e. the reset is always less than 264 line periods from the F1 pulse). With the LINE SELECT switch 'UP' the line counter will count to 526 before resetting. The number displayed by the display counter increases until 263. The next reset pulse is not after 526 counts, but is derived from the F1 pulse so that line 1 is displayed.

Similarly, when counting 'DOWN' the line counter resets after 524 lines. The number displayed decreases down to 001. The next reset pulse is the F2 pulse, resetting the counter at the end of field 1 again, so line 263 is displayed.

4. SELECTED LINES 15,16,17,18,19,20,21

An individual line, in Field 1 or Field 2 (or both) from line 15 to line 21 may be viewed by using the 7 appropriate positions of the VIDEO SELECT switch. These lines are generally of interest for viewing Teletext data and test signals which precede the main picture information. It is convenient to use the VIDEO SELECT switch for viewing these lines, instead of using the line slector display since instant access is available. The seven tapped outputs for these lines arrive at the DELAY trigger monostable from a ten stage Johnson type counter via the VIDEO SELECT switch. The counter has a feedback arranged on it so that it actually counts to 9 and then stops. It must be the reset before it can commence counting again. In common with the 525 line counter and the Display counter it is clocked by the delayed edge from the 50μs monostable multivibrator. It derives its reset from gated outputs from the 525 line counter which occur on counts of 10. The reset is held high until this count has occured. When the reset has dropped low the counter then commences clocking on the next clock, which corresponds to a count of 11 i.e. line 14. Since the counter is clocked about 50μs after the start of the 14th line of the selected field the Q1 output rises high about

10μs or so before the 15th line. Similarly, the Q2 output goes high before the 16th line and so on.

The timebase then gets triggered via the DELAY trigger monostable just prior to the start of the selected line.

5. FIELD SELECTION

The FIELD SELECT switch operates to select the field to be viewed in all the TV trigger modes except line repetitive. It works in different ways depending on the trigger mode. In FIELD trigger mode, the DELAY monostable is triggered directly by the field pulse (the narrow pulse between the 1st and 2nd broad pulse). The FIELD SELECT switch gates in either F1 or F2 or F1 added to F2, to give "field 1", "field 2" or "BOTH". The timebase is then triggered after the DELAY monostable resets.

In LINE 15–21 trigger mode, the FIELD SELECT switch gates different signals to the reset pin of the 525 line counter. These signals are, as before, the F1 or F2 or F1 added to F2 pulses. Thus, the 525 line counter is reset at the beginning of the field, and after 10 line counts resets the 10 stage Johnson counter. The chosen output is gated by the VIDEO SELECT switch to the DELAY monostable.

In the LINE SELECT trigger mode, the 525 line counter is reset independently of the field pulses, but always between the F1 pulse and the F2 pulse that follows it. With field 1 selected, the DELAY monostable is triggered after 521 line counts, i.e. during the following field 1. With field 2 selected, the DELAY monostable is triggered after 259 line counts, i.e. during the following field 2, and 262 lines before the equivalent line in field 1. If both fields are selected, the DELAY monostable is triggered after 259 and 521 line counts.

4.2 INPUT ATTENUATORS AND PRE-AMPLIFIERS

NOTE: The Attenuator and Pre-amplifiers in the CH1 channel are identical* to those in the CH2 channel. Accordingly, only the CH1 channel is described. Where a corresponding component carries a different number in CH2, this number is shown in brackets after the CH1 number.

* CH2 has no x5 gain facility but has fine/coarse shift control.

The input signal is applied from the front panel socket SKY to the 3 position level switch, S10. When the INPUT COUPLING SWITCH is in the DC position, the input signal is coupled directly to the Input Attenutaor stage. In the AC position, the input signal passes through C155. This capacitor prevents the dc component of the input signal from passing to the amplifier. The GND position opens the signal path and connects the input circuit of the amplifier to ground. This provides a ground reference without having to disconnect the applied signal from the input connector.

The input attenuators are frequency compensated, voltage dividers. For dc and low frequency signals they are primarily resistance dividers and the attenuation is determined by the resistance ratio, the effect of the capacitors being negligible. However, at high frequencies, the reactance of the capacitors decreases and the attenuator becomes primarily a capacitive divider. Each attenuator contains an adjustable series capacitor to provide optimum response for the high frequency components and an adjustable shunt capacitor to set up the input capacity of each section. The component values in each section are arranged to provide the required attenuation and present the same RC characteristic for all settings of the VOLT/cm switch.

Two attenuator sections are employed giving an attenuation of 10 or 100 respectively. These are used singly or cascaded. The basic amplifier provides a maximum sensitivity (for full bandwidth) of 5mV/cm; gain switching in the amplifier reduces this to provide the 10mV/cm and 20mV/cm settings. The x10 attenuator is introduced to provide the 50, 100 and 200mV/cm ranges; the x100 to provide the 500mV, 1V, 2V/cm ranges and the x100 and x10 cascaded to provide the 5, 10 and 20V ranges.

The x10 attenuator consists of R176 and R177. Capacitor, C165, adjusts the input capacitance on the 50, 100, 200mV/cm ranges, while C167corrects the frequency response of the attenuator.

The x100 attenuator consists of R163 and R169. Capacitor, C159, adjusts the input capacitance on 500mV, 1V, 2V/cm ranges, while C161 corrects the frequency response of the attenuator.

Capacitor, C171, provides adjustment for the input capacity when the attenuators are not in circuit. R187 determines the input resistance of the oscilloscope when the attenuators are not in circuit and contributes to the attenuating resistors on all other ranges.

The output from the attenuator is taken via the input current limiting resistor, R189, to the input stage consisting of the source followers, TR101 & TR102, with its current source, TR102. These FET's are matched and thermally coupled to minimize any drift due to temperature changes. The output from this stage is connected to the emitter follower, TR103, to provide a low impedance drive to the following stage. The second output from the pre-amplifier, the balance control voltage set by the front panel fine gain BALance, R11 (21), is coupled via emitter follower, TR104, to the next stage. Transistors, TR103 and TR104, are selected and thermally connected to minimize any drift due to temperature changes.

The output from the emitter followers is applied to the long-tailed pair amplifier, TR121 and TR122. TR120 being a constant current source of this stage. The stage provides a nominal gain of about 5, the emitter circuit however contains the FINE GAIN CONTROL, R10 (R20), which allows a reduction in gain of at least 2:5:1. When the fine GAIN CONTROL is switched out of the CALIBRATED position, S13 (S23) closes and the l.e.d., D123, is illuminated. The two transistors in this stage are matched and thermally coupled together in order to

reduce drift to a minimum. In addition,theyare mounted on the rear screen of the attenuator assembly in close proximity to the FINE GAIN CONTROL. This ensures that the length of the emitter leads to the gain control and consequently their inductance is kept to a minimum.

A potentiometer, R123, is provided in the emitter circuit giving some variation of the collector currents. This allows the emitter potentials of the following stage to be equalised to prevent trace movement when gain switching.

The collector supply is stabilised by the 5.6V zener diode, D121, giving a collector potential of +4V. This provides sufficient margin to allow for variations of input dc level due to the possible range of FET source to gate voltage.

The following stage is also a long-tailed pair with gain switching incorporated into the emitter circuit. In the minimum gain condition the gain is determined by the emitter resistors, R132 and R134. The gain is raised by x2 and x4 by connecting between the emitters network, R137 and R138, or network, R135 and R136 respectively, with the two trimmers, C122 and C123, providing a high frequency compensation to equalize frequency response between ranges. Decoupled resistors, R154 and R155, are added to reduce collector dissipation and keep drift due to thermal effects to a minimum. The collector supply is stabilized by the5.6V zener, D122.

The final stage on this board and on the attenuator assembly is a pair of emitter followers, TR125 and TR126.

The trigger signal is taken directly from the emitters but the signal for the remainder of the Y amplifier is tapped down the emitter loads by the addition of a small series resistor. This allows a dc shift of the output to be provided for, balancing in the following stage by the addition of the potentiometer, R146, in the bottom end of the emitter loads.

The signal outputs from this stage represent approximately 25mV/cm of screen deflection, the dc level being nominally +7.5 volts.

The signals are then passed to the Beam Switch printed circuit board, in the case of CH1 direct, but in the case of CH2 via the INVERT SWITCH, S201.

4.3 BEAM SWITCH

The CH1 and CH2 signals feed to the beam switch printed circuit board into two identical long-tailed pair amplifiers, TR203/4 and TR205/6. Each amplifier provides a number of additional functions, namely:

1. SHIFT CONTROL is obtained by means of potentiometers, R26 and R27, in series with the emitter resistors of each stage. R37 provides Fine Shift on CH2.
2. Overall gain adjustment of each channel is provided for by means of the two networks, R226/R227 and R231/R232.
3. The maximum sensitivity of both CH1 and CH2 channels can be increased to 1mV/cm, this requires that the gain of these stages is increased by five times and is achieved by shunting across the emitter circuit the network, R228/R229, for CH1 and R233/R234 for CH2. The switch for this function is mounted on the rear of the respective shift controls.
4. Networks, R230/C202 and R235/C206, are included to allow the h.f. response of the two channels to be matched.

The signals from this pair of amplifiers are fed to the beam switch circuit consisting of eight diodes, D201 to D208, inclusive. The switch is operated by signals applied in anti-phase to points 26 and 29 from the Beam Switch bistable. The signal level at these points switches from approximately +7V to approximately +0.3V. Thus when point 26 rises to +7V diodes, D201 and D202, are cut-off and diodes, D203 and D204, are turned on, allowing CH2 signals to pass to the following stage. At the same time, point 29 will be at approximately +0.3V, allowing D205 and D206 to conduct and prevent CH2 signals reaching the following stage. When the potentials on points 26 and 29 reverse, CH2 signals will pass to the following stage and CH1 signals will be blocked.

The output from the beam switch network is taken to transistors, TR210 and TR211, connected as shunt feedback amplifiers with R249 and R250 providing feedback from the collector to base of the respective transistor. Provision is also made in this stage by means of A.O.T. resistors, R294/R295, to take out small unbalances which cause excessive trace movement when switched to the ADD mode. Also in the ADD mode it is necessary, since two stages are now connected to a common load, to remove half the resultant current in the load, this is achieved by returning R245 and R246 to the −15V line when switching to ADD.

Signals from this stage pass to the delay line driver, a further long-tailed pair, TR212/TR213, fed from a constant current source, TR214. A current of 10mA per side is common to this stage and, via the delay line, to the delay line terminating stage.

The Beam Switch bistable consists of transistors, TR215 and TR216, the conducting stage of these determining which channel is displayed. For single trace operation, either of the emitters is grounded via points 35 and 36. For dual trace operation, both emitters are grounded and the transistors are turned on or off by pulses from TR217 routed via capacitors, C213 and C218, and diodes, D212 and D211. In the ADD mode both emitters are open circuited raising both collector voltages and hence opening both diode gates.

The chop multivibrator contains transistors, TR217 and TR218, which operate as an emitter-coupled astable multivibrator, whose frequency of approximately 500kHz is determined by R280, R285 and C221.

In addition to operation for the chop function, the circuit acts as a monostable when the alternate mode of beam switching is selected. In the alternate mode, the circuit produces 1 pulse per timebase sweep and is fed with an

end-of-sweep pulse from the timebase bistable. The -15V volts supply is connected to point 32 via the FUNCTION SWITCH, this increases the current through TR218 and causes a drop in the level of the collector voltage.

This drop cuts off TR217. The negative-going end-of-sweep pulse thus finds the circuit in a monostable condition which it triggers, producing a high amplitude positive-going pulse at the collector of TR218 and a negative-going pulse at TR217. The output from TR218 is taken to the Bright-up Amplifier to blank the trace during the chop transition period and that from TR217 to the Beam Switch bistable.

4.4 DELAY LINE AND DELAY LINE EQUALISER

The Delay Line is of the wound type and introduces a signal delay of approximately 95ns. This time allows for delay in the timebase and bright-up circuits and ensures that the first part of a signal is visible.

The output of the delay line is terminated by the resistors, R301 and R302, and feeds into the common base stage, TR300 and TR301.

The Pulse response compensation for the delay line is provided in the following stage, TR302/TR303, by means of resistance/capacitor networks, R308/C302, R309/C303, R310/C305, R311 and C306, connected between the emitters.

A further stage, TR304/TR305, provides additional frequency compensation (C310, C311, R324/C312) and raises the signal to the required level to drive the output stage.

4.5 OUTPUT STAGE

The output from TR304 and TR305 feeds the grounded base pair, TR356 and TR357. From this stage the signal drives into the differential input pair, TR351 and TR352. These two transistors, together with TR353 and TR354, operate a differential cascode amplifier.

The collector loads are made up of two resistors in series in order to give the required dissipation with minimum stray capacitance. High frequency compensation is provided by the inductances, L351 and L352.

A constant-current transistor, TR355, gives a current in each side of the output stage of approximately 25mA and holds this stable against small variations of the dc input level of +2.4V. At this current the nominal mean Y plate potential is +75V.

4.6 Y TRIGGER AMPLIFIERS AND CH2 OUTPUT AMPLIFIER

Incorporated on the Beam Switch printed circuit board are the CH1, CH2 and composite, trigger amplifiers and the CH2 output amplifier stage.

The CH1 and CH2 trigger amplifiers consist of long-tail pairs, TR201/TR202 and TR207/TR208, receiving differential signals from the CH1 and CH2 pre-amplifiers and providing single ended output for the timebase.

R213 and R223 provide a means of setting the dc level for the trigger circuits (nominally 0V).

In addition a further output is taken from the CH2 trigger amplifier and fed to an amplifying and inverting stage, TR209. This provides an output level of 100mV/cm and when used in conjunction with the X amplifier, gives an X-Y operation facility.

The gain of this stage can be set by R238 and phase shift correction is provided by C228 connected across the feedback resistor, R242.

4.7 TRIGGER SELECTION AND AMPLIFICATION

Trigger sources (CH1, CH2, TV, LINE, EXT.) are taken to S40AF. The internal trigger signals are brought via 50Ω coax, and are terminated by R400, R406 and R577. TV trigger signals are derived from the Delay Monostable, IC617a, and attenuated by R725 and R577. The Line trigger signal is provided from a single turn secondary winding on the mains transformer and the correct trigger voltage is obtained by the simple attenuator, R405 (mounted on S40), and R773 on the main TV logic board. External trigger signals are attenuated approximately fifty times by the network R401, C400, R402 and C401. The signal selected by S40AF is passed via the trigger coupling switch, S42, to two cascaded-emitter-follower stages, TR409 and TR410. D406 and D407 provide the necessary protection against excessively large external trigger signals. The signal from the emitter of TR410 is switched by S40BF and S40BB according to the selected trigger slope, to the base of TR413 or TR414, which form a long-tailed pair amplifier. S40BF, S40BB also connect the undriven base of this amplifier to the network, C451, R437 and R438 which provides a low impedance path to ground for high frequency signals and the correct bias to balance the amplifier. The trigger level control (R440) also acts on this network via R441, introducing a positive or negative offset, which is thus mixed with the amplified trigger signal.

The network, R557, C454 and C415, between the emitter of TR413 and TR414, provides high frequency compensation. The output from TR414 is applied to the base of TR415 which together with TR416 forms another long-tailed amplifier, R488. R490 determines the gain and C424 provides high frequency compensation. The base of TR416 is normally held at a fixed bias by zener diode, D423, except when S41b (the auto level switch) is open (see Auto operation). When the level control (R440) is adjusted so that the base potentials of TR413 and TR414 are equal, R453 adjusts the dc potential on the base of TR415 so that the Schmitt trigger circuit is brought near its switching point, maintaining the same trigger level for positive and negative slope selection.

The output from the collector of TR415 is taken via

D402 and R571 (see trigger signal routing) to the grounded-base amplifier, TR404, and from the collector of this transistor via D401 to the Schmitt trigger circuit. The output from TR416 collector is connected to the auto level circuit.

4.8 AUTO

When auto is selected by turning the 'A' trigger level control to its extreme anticlockwise position, S41a and S41b open. R491 and the base of TR416 are disconnected from the zener diode, D423, so that the dc potential set by R453 has little effect on the amplifier, TR415 and TR416. The opening of S41 causes the potential at the extreme anticlockwise end of the level control to change from −15V approx. to 0V approx. (R440 and R552 form a potential divider across the ±15V lines.) Thus the amplifier, TR413/TR414, is still approximately balanced. S41a also operates on TR403 (see Trigger signal routing) to energise the bright-line circuit. (See free run and bright-line circuit.) Trigger signals from the collector of TR416 are coupled via C411 and C412 to the bases of the complementary amplifier stage, TR406 and TR407. Emitter resistors, R426 and R427, define the gain, and C442 and C443 provide high frequency compensation. Both transistors are normally biased off but are sensitive to small input signals with one or the other being turned on. The output resultant from the commoned collectors is an amplified form of the input whcih is not paralysed by inputs of widely differing mark/space ratio. It is applied via D416 to grounded base stage, TR404, and thence to the Schmitt trigger.

4.9 TRIGGER COUPLING

The selected trigger signal is taken to the coupling switch, S42, where a simple filter is connected into the signal path on all modes except dc coupled. In the ac connection, C402 removes the dc component. In the HF reject mode the time constant of R407, C466 rolls off the response of the amplifier to high frequency signals. In the LF reject position the trigger signal is coupled via the small value capacitor, C403, whose impedance at low frequency forms an effective attenuator with the input resistor of the trigger amplifier to LF signals.

4.10 TRIGGER SIGNAL ROUTING

The different trigger circuit connections, manual or auto trigger, are controlled by the state of TR403/TR405, and the position of the trigger coupling switch, S42. In manual operation, S41a is closed and with no voltage across its base resistor, R552, TR405 is cut off. Current through R420 and R421 turns on TR403 causing its collector potential to become approximately 15V. Current through R424 and D410, pulls the collector potentials of TR406 and TR407 negative, cutting off D416, and disconnecting the auto circuit output from the grounded base amplifier, TR404. Current through R418 acts on the bright-line circuit (see Free run and bright-line circuit), to prevent it operating. Trigger signals from TR415 are passed to the Schmitt trigger as current from TR415 flows through D402 into TR404, and from the collector of TR404 via D401 to the Schmitt trigger.

When Auto is selected S41a is open, base current through R552 bottoms TR405, and this in turn cuts off TR403. Current through R408 and D435 causes the collector of TR415 to go negative, cutting off D402. At the same time, the current through R424and D410 is removed allowing the collector potentials of TR406 and TR407 to rise, turning on D416. Trigger signals now pass from the collector of TR416 to the auto circuit, TR406 and TR407, and then via TR404 to the Schmitt trigger. Also, when TR403 is cut off, current through R418 is removed, energising the bright-line circuit, TR411 and TR412, and diode, D404, is turned on by current flowing through R422 enabling the Schmitt trigger output waveform to drive C407. (See Free run and bright-line circuit.)

4.11 SCHMITT TRIGGER

This consists of TR401, TR402 and associated components. When the base of TR401 is negative with respect to ground, TR401 is off and TR402 is on.

R471 and R416 bias the base of TR402 about 0.5 volt positive. When the base voltage of TR401 is driven positive it will start to conduct. R416 provides positive feedback causing a rapid transition to the opposite state with TR401 conducting and TR402 cut off. When the base of TR401 returns negative, the switch-over will occur at a lower level because of the change in potential across R416. This backlash prevents the trigger from responding to low level noise when biased to its operating point.

C404, R414 and C405 provide high frequency compensation of the feedback network. The output from the collector of TR401 is taken via D404 and C407 to the bright-line circuit.

Trigger pulses are applied via C420 to the shunt feedback amplifier, TR438, with R470 as the gain defining resistor. C420, R470 form a differentiating network such that pulse edges appearing on the output of the Schmitt trigger result in positive and negative impulses appearing at the collector of TR438, and these are applied via R467, C423, D420, to one input of the timebase bistable. TR437, connected between base and emitter of TR438 is activated by the hold-off circuit (see section4.14 HOLD-OFF).

BRIGHT-LINE AND FREE RUN

The bright-line circuit detects the absence of Schmitt trigger pulses and applies a dc trigger to the ramp bistable. It operates only when the AUTO function is selected. S41a opens,turning TR405 on, which applies a small forward current to D404. If no trigger pulses are present the emitter of TR412 is at approximately −3V, holding TR417 off, allowing current to flow via R574, R472, to the input of the shunt feedback stage, TR438, driving its output low, acting as a dc trigger on the ramp bistable.

A negative transition of the collector of TR402 is transferred by D404, C407 and D415 to the base of TR411. As this transistor turns on, the rise of its collector potential is transferred via TR412, D418 and C418, in a regenerative loop to its emitter, so that TR411 bottoms, and the emitter of TR412 follows. The regenerative action then ceases and TR411 is turned off, but its collector potential falls slowly as C418 is discharged by R430. TR412 again acts as an emitter follower. However, the regenerative action caused by any trigger pulse can be initiated at any point in the discharge of C418, and when the timebase is being triggered at medium and high frequencies, the system is permanently biased in the condition which allows normal triggered operation.

4.12 TIMEBASE BISTABLE

TR419 and TR420 form the emitter-coupled trigger bistable. R470 normally biases on TR419 and the low potential across R479 holds off TR420.

A negative transition from the Schmitt trigger is coupled via C420 and D420 to turn on TR419. The positive movement of the collector of TR419 is transferred by R479 to hold on TR420 and the bistable is reversed.

The collectors of TR421 and TR422 provide the two buffered outputs from the bistable. TR421 provides the bright-up current pulse to the bright-up amplifier. The alternate beam switching pulse is provided from TR422 via C432 and emitter-follower, TR430. When TR420 is turned on, its collector potential falls and the diode, D422, conducts to initiate generation of the ramp as described in section 4.13. The effect is that the emitter of TR432 goes negative until D431 is brought into conduction when TR420 is turned off and the bistable reverts to its initial condition, ready for the next trigger pulse via D421.

4.13 RAMP GENERATOR

The basic ramp generator is the bootstrap feedback circuit formed by FET, TR426, as a source-follower with two subsequent emitter-followers, TR427 and TR428. The base-to-emitter voltages of these two transistors are approximately equal and opposite so that the emitter of TR428 follows any change of gate voltage on TR426 with an offset which is the gate to source voltage of TR426, plus the potential across R514. The current in TR426 and hence the voltage between its gate and the base of TR427 is held constant, independent of actual potential as this current is the collector current of the grounded-base transistor, TR435.

Consequently there is a constant voltage across the selected timing resistor, Rt, which in the absence of other influences, flows to ground through the selected timing capacitor, Ct, causing the voltage across this capacitor to drop linearly. This linear ramp appears similarly on the emitter of TR428, is transferred to the emitter of TR432 and goes via the diode gate, D432 and D433, to the X gate. It is also tapped off via R547 to the ramp output amplifier, as described in section 4.22.2.

The sweep speed, that is the ramp slope, is determined by the values of Ct and Rt which are selected for a particular range. Details of this range switching are shown in Fig. 5.

The third factor to control the sweep speed is the gate-to-source voltage of TR426. This FET is matched in characteristics with TR425. As both devices carry the same current being coupled via the grounded base transistor, TR435, and as R512 is equal to R514, the voltage between the gate of TR426 and the base of TR427 is equal to the voltage between gate and source of TR425, plus the voltage across R512. The latter voltage sum is set by resistor network, R511, R508 and R509, together with the preset calibration control, R510, and the variable sweep speed control, R507. When the variable control is moved from the CALIBRATED position, S74 closes enabling the led, D441, to light.

During the flyback period when the timebase bistable is reset, D422 is biased off and current flows through R540 into the emitter of TR431 and so to D429. This current is much greater than the current through Rt, so that the timing capacitor, Ct, is charged rapidly positive, and the emitter of TR428 follows until it approaches zero potential. At this point, TR429 conducts, diverting current from TR431. This subsequent reduction of the current in D429, limits when it balances the current through Rt. This is the quiescent point of the ramp generator with the emitter of TR428 and the collector of TR435 approximately at zero, and the voltage on the gate of TR426 at +4V. When the timebase bistable is switched by a trigger pulse, D422 is turned on, removing completely emitter current from TR431 and reducing the current in D429 to zero. The normal ramp action then takes place with the constant current through the timing resistor, Rt, negatively charging the capacitor, Ct. The capacitor charges linearly until the emitter of TR432 is at about 4V, when D431 conducts to reset the timebase bistable and complete the cycle.

4.14 HOLD-OFF

Triggering of the timebase bistable must be prevented or held-off during the flyback period until the ramp generator has fully returned to its quiescent state. When a trigger pulse switches the timebase bistable, TR419/TR420, the collector potential of TR419 goes positive and, acting through R448, turns TR437 on, presenting a low impedance path to ground to inhibit trigger pulses through C420. The capacitor, CH0 (representing the next smallest timing capacitor in the timing series Ct) is charged negatively by the negative-going ramp on the emitter of TR432, via gate, TR423/D425/D426. TR423 is only turned on by the timebase bistable during the sweep, via R481, and ensures that CH0 starts to charge immediately the ramp is initiated.

As CH0 charges negative, TR418 is cut off and the current in R466 flows through R458 to cause TR437 to conduct. At the end of sweep when the timebase bistable is reset, TR423 is cut off, removing the charging current from

CH0. Current through R468 slowly discharges CH0.

While the sweep generator is in its flyback period, CH0 holds TR418 cut off, leaving TR437 in conduction to inhibit trigger pulses into the timebase bistable. After the ramp generator has reached its quiescent condition, CH0 discharges sufficiently to allow TR418 to conduct and cut off TR437, allowing D420 to conduct on the next trigger pulse to initiate another sweep.

4.15 SYNC SEPARATOR SYSTEM

1. INPUT AMPLIFIER

Video in from the front panel attenuator switch at normal amplitude, 0.5V p-p is ac coupled to emitter follower TR600. Since this stage has a high input impedance, the 75Ω termination for the input attenuator is provided by R603, R604 and R608 on the front panel switch. The video signal from TR600 emitter passes to the amplifier, TR607, TR608 and TR609. TR607 and TR608 form a long-tailed pair and TR609 is an emitter follower. Negative feedback is taken from TR609 emitter to TR608 base and the gain of the amplifier (about x6) is determined by the ratios of R649 and R650. Frequency response is controlled by the tuned circuit, L601, C614, C615 and filter, R653, C616. These components provide a progressive roll-off starting at 1.5MHz, with a notch at 3.6MHz. The amplifier is biased so that a certain amount of white-level clipping may occur.

2. CLAMP PULSE GENERATOR

Transistor, TR611, is fed composite sync, via the emitter-follower TR610, and functions as a sync separator. The sync pulses developed at TR611 may contain sound pulses (if a Sound-in-Sync signal is used). These extra pulses are removed by the action of TR615 which is driven into conduction during the sound-pulse period by a signal derived from the digit-blanking generator, IC603b, via inverter, TR625. The blanked sync pulses appearing at the collector of TR615 are differentiated by C621 and the negative-going edges are used to drive TR614 into cut-off. Thus the required positive-going clamp pulses timed to the Back Porch Period are developed at TR614 collector.

3. START-UP CLAMP

The output of the input amplifier is passed via emitter-follower, TR612, and ac coupled to the 'start-up' clamp, TR613. Positive-going pulses of duration approximately 2μs are applied to the gate of TR613, this causes it to conduct and clamp the signal to earth potential. Clamping occurs at black level during the Back Porch. The function of this clamp is to ensure that the main clamp locks initially to the correct part of waveform. The main clamp relies on an output signal from the complete sync separator and after start-up provides the major part of the clamping action.

4. MAIN CLAMP

The main clamp follows on from the start-up clamp, TR613, the signal is passed via C619 and R663 to the emitter-follower, TR618. The FET, TR619, is turned on by a positive-going pulse on its gate. This causes the video signal to be clamped to zero volts during the Back Porch. The main clamp pulses are derived from the comparator, IC602, via inverter, TR624. Line sync pulses are inverted by TR624 and then differentiated by C635. Negative spikes from the back edge of syncs are then used to turn TR616 off so as to produce a positive-going clamp pulse at its collector and so switch on FET, TR619, during the Back Porch.

5. SYNC SEPARATION

The clamped video present at TR618 emitter may contain sound pulses in the sync-period (with a Sound-in-Sync signal). These sound pulses are removed by the action of TR621 before sync slicing takes place. During line-sync periods TR621 is driven into conduction by a positive-going pulse obtained from the digit-blanking generator, IC603b, and the sound pulses so gated out. Because TR621 continues to operate during the field blanking period alternate equalizing pulses are increased in duration to 4μs.

Integrated circuit, IC602, is a differential comparator which functions as a sync slicer. The device compares the sync-pulse amplitude of the clamped video signal with a dc reference signal which has half the amplitude of syncs and is derived from the sync-level detector. When the input syncs on pin 2 go more negative than the reference level on pin 3, the output on pin 7 goes negative and thus negative-going sync pulses with a peak-to-peak amplitude of 3.5V are developed. These pulses are fed via a buffer, IC601b and c, to the mixed sync output of the sync separator, and to the 'SYNC' front panel monitor point via R643.

6. SYNC-LEVEL DETECTOR

The clamped video from the emitter follower, TR618, is fed to TR617. This transistor conducts during sync pulse periods and charges C625 to a potential proportional to the peak sync-pulse amplitude. Smoothing is carried out by R673 and C624. The emitter follower, TR620, removes the base emitter offset caused by TR617. The resultant dc signal is then fed, via a potential divider network, R676, R677, which reduces it to half sync amplitude, to the sync slicer, IC602.

7. DIGIT BLANKING GENERATOR

Separated sync pulses from IC602 are fed via a buffer, IC601, to the input of a monostable, IC603A. The time constant of IC603A is approximately 50μs. This is longer than half a television line and so prevents the generation of unnecessary blanking pulses at twice-line frequency during the field-sync period. The monostable triggers on the leading edge of syncs.

The output of monostable IC603a at pin 7 is then fed to monostable IC603b, pin 11. This monstable generates line-frequency pulses with a duration of 4.5μs. These pulses are used as digit-blanking pulses (from pin 10 via TR621) and after inversion by TR625 as the main clamp pulses.

8. FIELD-PULSE SEPARATION

Negative-going mixed sync pulses from IC601c, pin 6, are fed to the base of TR626 via R691 and C637. The time-constant of C637, R692, is so arranged that the line-sync pulses do not affect the cut-off state of TR626. However, during the longer duration broad pulses in the field synchronizing period, C637 charges sufficiently through R692 to turn on TR626 on the narrow (2.3µs) line sync pulses which follow the broad pulses. The negative-going pulses on TR626 collector charge capacitor C638 such that the first pulse at IC601d input, pin 9, is the largest in amplitude. This is because successive pulses must await the discharge period of C638 via R693 before further charge can be transferred to IC601d. The output of IC601d is a positive-going pulse approx 1.8 s wide corresponding to the gap between the first and second broad pulse.

9. FIELD IDENTIFICATION

The field pulse at IC601d, pin 8, occurs once on each field, during the narrow-line sync pulse period between the first and second broad field sync-pulses. IC603a produces a 50µs pulse at pins 6 and 7 commencing at the leading edge of each line sync pulse. Since the phasing of the first broad pulse shifts by half a line (32µs) on alternate fields, the 50µs positive-going Q output of IC603a, pin 6, will only coincide with the field pulse derived from IC601d, pin 8, on EVEN fields. Similarly, the Q output of IC603a at pin 7 will only coincide with the derived field pulse on ODD fields. The AND gates, IC605d and IC605c, detect the coincidences and produce negative-going pulses corresponding to Field 1 (EVEN) and Field 2 (ODD). (See waveforms, Fig. 12.)

10. GENERATION OF LINE RATE CLOCKING SIGNALS FOR COUNTERS

The 50µs square wave signal from IC603a, pin 6, is fed to IC617b which is a monostable triggering on the negative edges of the incoming square wave and so producing 5µs wide pulses to its output. The position of these pulses relative to the incoming video is about 50µs after the leading edge of the line sync pulses. A positive-going pulse output from this monostable is fed to IC606, pin 14, to provide the decade counter with positive clock edges. The negative-going pulse output from IC617b, pin 9, is taken to the 525 line counter, IC403, and the latch, IC401a, which operate on negative clock edges.

4.16 VIDEO SIGNAL SYSTEM

1. INPUT ATTENUATOR

The 'video in' from the front panel BNC socket passes to a 3-way input attenuator switch, S606, each sensitivity position is capable of input level variations of ±6dB. For a normal input level of 1V p-p the attenuator switch selects a 6dB pad formed from R600, R601 and R602, the 75 ohms termination for the pad is R603, R604 and R608. This gives an input impedance to the unit of 75 ohms irrespective of attenuator switch setting. The 2V input sensitivity setting is selected using the 12dB pad, R605, R606 and R607. The 0.5V sensitivity setting is a direct feed from the input socket to the termination (R603, R604, R608).

The signal feed to the clamp circuit is at a nominal level of 0.5V p-p and is ac coupled from the input termination.

The 'clamp out' signal to the display switch, S601, is taken from the junction of R603, R604 at a nominal level of 0.25V p-p. A small amount of frequency compensation is provided by the capacitor C611 shunting R604.

2. SIGNAL CLAMP

The input to the signal clamp is ac coupled from the input attenuator to the emitter follower, TR600, at a nominal level of 0.5V p-p. The signal then passes to a clamp utilizing a dual FET, TR601 and TR602. These are connected in a totem pole configuration with TR602 acting as a constant current source for the source follower, TR601, which provides a low impedance input at the base of TR603. This potential is adjustable by means of R617, the 'set clamp dc' preset control. Black level clamping at a time corresponding to the CSC burst occurs at TR601 gate due to the action of TR606. The FET, TR606, is turned on by positive-going line rate pulse derived from monostable IC600a and which is triggered by the back edge of mixed sync pulses from pin 6 of IC601c. The chrominance information is maintained during clamping by the tuned circuit L602, C606, C607. This is tuned to colour subcarrier frequency by adjustment of C606.

3. OUTPUT AMPLIFIER

The clamped output is passed to the output amplifier, TR603, TR604, TR605. This consists of a long-tailed pair followed by an emitter follower, TR605. Feedback is taken from TR605 emitter to the base of TR604 via R627 and R626. The gain can be preset by R628 with C605 compensating for the frequency response. Choice of R625 enables the output dc potential at TR605 emitter to be set to 0V.

The clamped signal output at TR605 emitter is at a nominal level of 1V p-p. This signal is fed to the video amplifier comprising TR633, TR634 and TR636, which modulates the crt via the Z mod input socket. A portion of the signal at TR605 emitter is attenuated by R632, R635 to give a 0.25V p-p signal which is fed to the 3-way DISPLAY SELECT switch, S601, and then to the 'video out' front panel BNC socket via the 'CAL' push button switch, S603.

4. VIDEO OUTPUT

The 'video out' BNC socket is coupled normally via a short cable to the high impedance CH2 input of the oscilloscope. The input coupling should be set to dc and the sensitivity to 50mV/div. The signal at the 'video out' socket is at nominal level 0.25V p-p which gives a 5 division vertical display on the oscilloscope.

When the 'CAL' button is operated a 0.25V p-p square wave appears on the display. This should correspond to the same amplitude as obtained from a 1V p-p video signal when the video attenuator is switched to 1V (0dB) position. If the display function switch, S601, is switched to 'Picture' a field ramp waveform is routed to the display and at the

same time a line-rate ramp replaces the normal X-deflection timebase output. This produces a 525-line raster on the oscilloscope.

4.17 TV TRIGGERING SYSTEM

1. TV TRIGGER SELECTION AND DELAY

TV triggering is controlled by means of the 10-way front panel VIDEO SELECT swithc, S602, and the mains TRIGGER SELECT switch, S40. This latter can be set to "TV" or "OVERLAY". The time by which the trigger is delayed is set by the multi-turn DELAY potentiometer, and in OVERLAY mode this is combined with the undelayed trigger pulse just before the line sync pulse.

The selected trigger signal, from the VIDEO SELECT switch, is routed to the Delay monostable IC617a. The time constant of the monostable is variable between about 4μs and about 90μs by the "DELAY" control. Its outputs are fed via the gates of IC630 to the TRIGGER SELECT switch, IC630 is arranged to give a negative-going pulse in TV mode and alternately negative and positive going pulses in OVERLAY mode. Thus, in TV mode, the timebase triggers on the delayed edge, while in OVERLAY mode it triggers alternately on the undelayed and the delayed edge. Pin 6 of the monostable also goes to TR635, via R749 to provide bright-up on the raster display, thus indicating the position of the DELAY control in PICTURE mode.

2. 525 LINE COUNTER

IC403 is a twelve stage binary counter (2 stages are not used). In all positions of the VIDEO SELECT switch except LINE SELECT, IC403 is reset to zero by the field pulse (F1, F2 or F1 plus F2) selected by the FIELD SELECT switch. The line counter is clocked by line rate pulses from IC617b and counts to 525 before being reset again by the field pulse (in the "BOTH" fields mode it is reset at every field and counts only to 262 or 263).

3. FIELD TRIGGERING

Even and odd field trigger pulses, F1 and F2, coincident with the gap between the first and second broad pulse are routed to the DELAY monostable via gates IC412a and 412c and IC410b and IC413b which select the appropriate pulse according to the position of the FIELD SELECT switch, S604.

4. LINE REP TRIGGERING

LINE REPETITIVE triggering actually operates on alternate lines and the signal is derived from the 625 line counter, IC403. In this mode the counter is reset by the selected field pulse and the LINE REP trigger pulse consists of the Q0 output of the counter, which effectively divides the line frequency by two, so providing trigger on every other line. This enables the DELAY control to take up more than one line period of delay, providing an overlap into the next line if required.

LINE REP triggering may ber used on a generator without field sync information, and under these condition, the counter, IC403, receives no reset pulse but simply works as a divider.

5. LINE 15–21 TRIGGERING

In this mode, the 525 line counter is reset, as usual, by the selected field pulse, via IC409 gating. The specified lines on the VIDEO SELECT switch are from 15 through to 21, in the field selected by S604. IC407a detects when the counter reaches a count of 10 and latches IC408c. The latch resets the 10 stage counter IC606 so it can be clocked by the line rate pulses from IC617b.

The 525 line counter is reset by the field pulse and clocked 50μs after the line sync pulse. It therefore receives its first clock pulse 50μs after the start of line 4. The 10 stage counter is therefore reset 50μs after the start of line 13 and its outputs Q0, Q1, Q2, etc. appear before the start of lines 15, 16, 17, etc. The output selected by the VIDEO SELECT switch goes to the DELAY monostable, to trigger the timebase. When IC606 has counted to 10 it stops counting until reset

6. LINE SELECTOR

When this mode is selected by the VIDEO SELECT switch, the trigger point of the timebase is controlled by the LINE SELECT toggle switch, S605, with the LED display indicating the line selected. IC403 functions as a free-running 525 line counter. It is not synchronized by field sync pulses. With S605 in the 'UP' position, the count changes to 526, and in the 'DOWN' position it counts to 524. This shifts the phase of the line counter by one step at a time with respect to the incoming 525 line video signal, incrementing or decrementin the line number shown.

The 525 line count is detected by the 4 input NAND gate IC410d and IC402a. It has 3 inputs from IC403, corresponding to Q2, Q3 and Q9. Its 4th input is driven from the combination of gates IC405c, IC405d, IC404a, b, c, d, IC410c, IC413a, IC409a. These select Q0 normally to give a count of 525, or Q1 for 'UP' to give a count of 526, or a logic high for 'DOWN' to give a count of 524, from IC402a. When the line counter has reached the required count IC402a generates a narrow pulse which is routed through to reset the line counter, IC403. IC409b,c, &d is a multiplexer which selects which pulse should reset the 525 line counter: the pulse after 525 line counts in LINE SELECT mode, or the field pulse in all other modes.

When displaying line 263 and wanting to count 'UP' or when on line 001 and wanting to count 'DOWN' the reset pulse must remain in the same field (i.e. field 1) rather than moving into the next field. This is ensured by IC415a and c which detect whether the reset pulse is going to be during the F1 period or F2 period. If it is going to be in the F1 period, the reset pulse is let through. If it is going to be in the F2 period, then the 525 line counter must be brought back to the other end of the F1 period. Thus, when counting 'UP' from 263, F1 pulse resets IC403 to the start of field 1, when counting 'DOWN' from 001, F2 pulse resets IC403 to the end of field 1. The multiplexer IC416b, c & d selects either the

normal reset pulse of the field pulse as selected by multiplexer IC416a, IC417a, c.

7. ADJUSTMENT OF LINE COUNT 'UP' AND 'DOWN'

When the LINE SELECT switch S605 is toggled either 'UP' or 'DOWN', IC410a removes the reset from the decade counters IC406 and IC411. These counters are clocked when IC403 is reset and so count the number of elapsed frames. After two such clocks Q2 output of IC406 goes high. This changes the function of gates IC404a, b, c, d, 409a, 410c, 405c, d, so that instead of letting through the Q0 output of IC403 its output depends on the position of S605. In the 'UP' position it lets through the Q1 output of IC403, and in the 'DOWN' position the output is always high. This makes IC402a count to 526 or 524 respectively (because its other inputs are from Q9, Q3 and Q2 of IC403). When IC403 is next reset, Q2 of IC406 goes low, and IC402a counts to 525 again. Q2 goes high after a further 9 clocks, so the line counter counts to 525 except for once every 10 frames. After 40 frames, IC411 has been clocked four times, and its Q4 output goes high. This disables the clock inputs to both IC406 and IC411, so IC401c output is permanently high, and IC403 is reset on the count of 524 (for 'DOWN') or 526 (for 'UP') at every frame, until S605 is released.

The overall effect is that, on operating the LINE SELECT switch, S605, there is a pause of 2 frame periods, then the count changes once every 10 frames for 40 frames, then at every frame from then on.

8. LINE SELECTOR DISPLAY

The LED display, IC621, indicates the line selected and is controlled by the counter/latch, IC620. A positive-going EVEN field pulse from IC605b resets the display counter/latch and the flip-flop IC401b and d. This pulse occurs half-way along line 4, field 1. When the flip-flop is reset by the reset pulse for IC403, IC401a is enabled, letting through the clock pulses from IC617b. These pulses are 5µs wide and occur 50µs after the leading edges of line sync signals. When the 525 line counter is reset, IC401a is disabled, preventing the line rate pulses from clocking IC620, and the Latch Enable input of IC626 goes high, holding the contents of the counter in the latch, and allowing the LED display to show the recorded line count.

9. FIELD SELECTOR SWITCH

S604 is an on-off-on toggle switch. It operates on the multiplexer IC412a, c, 410b, to select either F1, F2 or F1 plus F2 pulses. The selected pulse is sent directly to the DELAY monostable in FIELD trigger mode, or to reset the 525 line counter in LINE REP, and LINE 15–21 trigger modes, thus synchronizing the line counter to the required field (in LINE REP mode the field pulses are, in fact, irrelevant).

In LINE SELECT mode, the FIELD SELECT switch acts on the multiplexer IC407b, c, d, to select a count of either 521 for field 1, or 259 for field 2 or 521 and 259 for 'Both'. Because the field pulse F1 occurs during line 4 of the following EVEN field, a delay of 259 gives line 1 of the following ODD field.

4.18 PICTURE OPERATION

When 'PICTURE' display is selected the DISPLAY SELECT switch, S601, provides a +24 volt supply to the Line and Field ramp generator circuits and also to the Picture Drive output amplifier. This supply is derived from the 190 volt rail supply using the dropper resistors, R742, R743, and the zener diode, D610.

1. LINE RAMP GENERATOR

Line-rate pulses from IC603b, pin 9, are used to switch TR638 via C673 and R761, which discharges C674. TR639 is a constant current generator which charges C674 thus producing a line ramp at TR640 base. The resistor R759 is used to adjust the ramp amplitude. The emitter follower, TR640, feeds the dc restorer circuit, C675 and D613, and from there the ramp is connected to the x amplifier via the diode gate, D614, D615 and R767. (The wiring arrangement conveys the gated time-base ramp to the 'TV' timebase board before going to the x output amplifier via pin 12 on the output socket PLB.)

2. FIELD RAMP GENERATOR

Positive-going Field sync pulses from IC601d, pin 8, go to the Monostable IC600b, pin 12, which triggers on the leading edges and gives negative edge pulses of approximately 150µs duration at pin 9. This signal is used to charge C664 via R750 and the base emitter diode of TR637. TR637 is therefore switched on and discharges C665. At the end of the input pulse, R752 discharges C664, but not sufficiently to allow TR637 to turn on before the next input pulse arrives. Thus R752 effectively defines the base current of TR637. When C665 has been discharged by TR637 during the brief 150µs period, R753 and R758 provide an approximately constant current to charge C665 up again. A 2.5V ramp exists at the collector of TR637 which is attenuated by R758 and R753 to about 350mV and buffered by TR641 to provide the vertical Field ramp into the Y-amplifier. The signal is coupled by C668 to R754 and R755 which provide a dc bias on the ramp to centre the picture on the screen when the clamp amplifier is in use.

The DISPLAY SWITCH, S601b, connects the Field ramp to the Y amplifier input, via the BNC output socket on the front panel.

3. PICTURE DRIVE AMPLIFIER

A positive-going video signal of 1V peak-to-peak amplitude is fed from the clamp amplifier output (emitter of TR605) to the picture Drive amplifier input at TR633 base via the capacitor C657. TR633 is biased by R730 and R731 and acts as a direct coupled emitter follower into the common emitter amplifier, TR634. The output of TR634 is buffered by the emitter follower, TR636, to provide a negative-going video output of approximately 9 volts amplitude. HF peaking is provided by the network R734 and C658. TR635 is switched by the positive signal

from the trigger monostable, IC617a, pin 6, via R749 to provide bright-up on the picture to indicate the monostable trigger position.

After being fed through C659, the video output from TR636 is clamped at sync tips by D609 and the zener D620, to bias the modulation amplifier to the necessary level for handling the waveform. The video signal is connected to the rear panel PICTURE DRIVE output socket via L603 and R744.

4.19 EXTERNAL X AMPLIFIER

The circuit for the external X amplifier is included on the 'TV' logic circuit board. The external input signal is applied to the base of the amplifier transistor, TR647, through the capacitor/resistor network, C683, R791. The trimmer, C684, is used to set the HF response. The diode, D618, protects the base-emitter function of the transistor against excessive reverse voltage. Resistors, R790, R791 and R792, set the quiescent base voltage of the input transistor. Capacitor, C682, provides some HF peaking. The collector voltage swing is passed via the emitter-follower, TR648, through the diode, D619 (when the circuit is enabled), to the X amplifier. When External X is selected on the timebase range switch (S43) a +15V supply is sent to the DISPLAY SELECT switch (S601e). If this switch is not in 'PICTURE' mode, then the +15V supply is used to power the supply rail of the External X amplifier. When the amplifier operation is not selected R769 pulls this rail down to −15V to shut off the circuit.

4.20 X GATE AND X OUTPUT AMPLIFIER

The input of the X output amplifier can be connected to the timebase, the 'TV' ramp outputs or the output of the External X amplifier, as determined by the DISPLAY SELECT switch (S601), and the timebase range switch, S43.

The switching is performed by diode gates D432/D433 and D614/D615 for the timebase and TV line ramps respectively, and by D619 for the External X amplifier.

When External X is selected, and the DISPLAY SELECT switch, S601, is in either the 'CLAMP' or 'CLAMP OUT' mode, 15V is fed via S601C to R767 to cut off the gate comprising D614/D615. A second 15V supply via S601d cuts off the timebase gate D432/D433 via R549. The External X amplifier is then enabled by a +15V supply fed via S601e. Output from D619 is then fed to the X output amplifier.

When the timebase range switch is in any position other than Ext X, S601c and S601d, determines whether the TV line ramp or the timebase ramp is gated to the X output amplifier by applying +15V to either R767 or R549. R766 and R548 keep either gate off in absence of this voltage. Note that if Ext X is selected when the DISPLAY SELECT switch is in PICTURE mode, then the PICTURE mode is operative, since the Ext X +15V supply from S601e is not present. The X output amplifier consists of a long-tailed input pair (TR921 and TR929) driven from the current source, TR923. The inputs to the amplifier are the selected ramp/Ext X signal to the base of TR921 and the shift voltage to TR929. The output from this pair feeds via the emitter followers, TR922 and TR928, into the differential cascode output stage. There is overall shunt feedback to set the gain and stabilise the working conditions through resistors R923 and R949. The gain of the amplifier is set by the network, R927, and the preset R933, in the X1 mode. In the X10 mode the relay, RL921, is energised and contacts bring R938 and preset R943 into circuit.

4.21 CALIBRATOR

The components forming the calibrator circuit are mounted on the TV logic PC assy. The circuit consists of an emitter coupled multivibrator, TR644, and TR645, with C677 as the timing capacitor. The collector current through TR645 is used to turn on TR646 which supplies a switched current to a 6.2V reference zener via R779. The square waveform on the cathode of the zener is attenuated by the resistor chain R786, R787, R777 and R778. The potential formed across R777 and R778 is 1 volt peak-to-peak which is conveyed to the front panel output pin. The potential across R778 is 250mV peak-to-peak, which is switched by push button S603 to provide the TV calibration source.

4.22 THE BRIGHT-UP AMPLIFIER

The Bright-up amplifier which controls the Z modulation of the crt consists of an inverting amplifier, TR970, TR971 and TR972, with shunt feedback applied through R977, the base of TR970 being a virtual earth point. The inputs include current pulses from the timebase bistable via TR421, chop blanking current pulses from TR218, and external Z modulation current waveforms (from emitter-follower, TR903 and R974), a dc current derived from the INTENSITY control, R60, through R970, and a bias current through R971, obtained from the timebase DISPLAY switch circuit via R776, D612. The instantaneous sum of these input currents is balanced by the feedback current from the output through R977, so that the output voltage waveform follows the sum of the input currents.

The Intensity control current and the Ext Z modulation current are added through D970, the maximum intensity condition being when the current in D970 is zero, and the blanked condition being when the current in D970 is +2mA.

During the chop blanking period, a further +2mA current pulse is added which makes total applied input current >+2mA, and blanks the trace for all settings of the intensity control.

The maximum output from the amplifier is approximately 60 volts, corresponding to this 2mA change in input current. The diode, D971, ensures that when the amplifier is overloaded by a negative input, bright-up inputs do not move far from their normal working voltage.

Diodes, D974 and D975, ensure that TR972 does not bottom. TR971 provides essentially a high impedance constant current load for TR972 but C974 causes it to act as a complementary amplifier with TR972, to provide a low output impedance at high frequencies to drive the mainly capacitive load.

The output of the amplifier is connected via C979 directly to the grid of the crt, and through R982 to the low voltage end of the grid supply voltage doubler. The dc voltage with respect to ground applied to the grid, is then determined by the potentiometer, R988 (to allow for variations in grid cut-off between crt's), resistor, R987, across grid supply and the voltage on the output of the amplifier.

4.22.1 BEAM CURRENT LIMIT

Due to the high tube EHT used it is necessary to limit the crt beam current to prevent burning of the phosphor when the spot is stationary. Transistor TR904 is normally held on via R954 when no beam current is present, hence the emitter of TR905 is close to ground and no current is fed into the bright-up amplifier. The return current for the EHT multiplier flows through R954, as the intensity control is advanced TR904 is turned off, TR905 conducts feeding current to the bright-up amplifier, restricting the drive to the tube crt grid and limiting the beam current to approx. 1.5μA.

Under normal timebase operation when a ramp is present, diodes D904, D905 and C909 provide a positive bias to TR904, overriding the beam current limiting.

4.23 THE POWER SUPPLIES

The OS3350 basically operates from positive and negative 15V lines and a +190V line, each stabilised and independently protected against overload. The EHT lines are all obtained from a high frequency oscillator with overload protection but with direct stabilisation only on the −2kV crt cathode supply. This oscillator is supplied from the +20V unstabilised line used for the +15V line.

All supplies are obtained from transformer, T83, via the range selector switch, S81, the supply fuse, FS83, and supply on/off switch, S80.

One secondary from T83 is the 6.3V supply to the crt heater and another the low voltage (approx. .25 volt) for the line trigger signal. This latter voltage passes via SKB – PLB19 and PLB20 to the trigger selector switch. The three remaining secondaries are rectified and smoothed as follows.

4.23.1 +15V, −15 V and +190V LINES

One secondary from T83 feeds the bridge rectifier, MR83, and develops approximately 20V across capacitor, C85. This is used to obtain a stable, overload protected, −15 volt line using an integrated circuit regulator, IC801, which contains a reference, comparator input amplifier and output current amplifier. In addition it includes the overload protection circuitry to operate from the voltage developed across the current sensing resistor, R836. The output from this IC regulator drives the external series regulator, TR838.

The output of the line is set to be −15V by the preset potentiometer, R838. Components, R855 and C831, reduce the noise present on the internal reference and C832 gives feedback compensation to prevent oscillation.

A similar secondary from T83 is rectified by MR82 and develops approximately +20V across C84. Protected by FS832 this +20V supply feeds the EHT oscillator. The voltage across C84 is also used to obtain the stabilized +15 volt line.

TR833, TR834, TR835 and TR837 form the +15V stabiliser circuit, which is referenced to the −15V line. If the +15V line is not at the correct potential, the junction of the two equal resistors, R847 and R848, will not be at 0V. The resultant differential voltage between the bases of TR833 and TR834 will modify the collector current of TR833 to drive through TR835 to the series regulator element, TR837, and so correct the line potential.

Excessive current drawn from the +15V line will develop a potential across R835 causing D833 to conduct in turn limiting the base current to TR835 and so also that in TR837.

Fuses, FS833 and FS834, protect the +15 and −15 volt lines respectively.

Protection diodes, D835 and D836, are normally reverse biased and only conduct in the accidental condition of a short circuit between the +15V and −15V lines.

Diode, D834, protects the base-emitter junctions of TR833 and TR834 against excessive reverse voltages. Capacitors, C836 and C833, give hf roll-off to prevent oscillation; C835 reduces output ripple.

The secondary from T83 is rectified by MR81 and develops approximately 220V across C83.

R84 and C86 reduce the output line ripple. The +190 volt line is referenced from the −15 volt line by resistors, R842 and R843. Any error potential at the junction of these resistors drives the error amplifier, TR831, which in turn controls the series transistor, TR839. Transistor, TR832, protects TR839 from over voltage at switch-on, or in the event of failure of the −15V line. If the junction of the potential divider, R840 and R841, goes too far negative, TR832 conducts, allowing TR839 to conduct.

Short circuit protection on the 190V line is by means of the fuse, FS831.

4.23.2 EHT SUPPLIES

The EHT supply circuitry is as shown in Fig. 8. It comprises a single transistor, transformer coupled oscillator with a single tapped secondary to provide three lines of approximately −2000 volts, −2100 volts and +14kV, mounted together with an error amplifier within the EHT box assembly.

The tap on the transformer secondary feeds two voltage doubler circuits, that for the grid supply being formed by D804, D806 and C804, C805. The return path for the doubler circuit is via TR802. This transistor is driven from the bright-up amplifier and modulates the grid supply at dc and low frequencies. High frequencies are fed to the grid of the tube via C979. The second voltage doubler, D802, D803 and C802, C803, feeds the crt cathode via the 120V zener, this ensures that the grid is at least 120V more negative than the cathode, the actual value being set by R988 and allows for variations in crt cut-off voltage. The cathode supply voltage doubler return is via R816. Excessive tube cathode current turns TR805 on and reduces the drive to the crt. This effectively limits the available tube beam current and gives over-current protection to the oscillator (see also section 4.22.1). EHT stabilisation is achieved by feeding a small fraction of the cathode voltage to the error amplifier, TR803 and TR804, via R805 where it is compared with a feed from the stabilised +15 volt line on the power supply board. Transistor, TR803, varies the base drive to TR801 so controlling the collector voltage and hence the dc output.

Additional over-current protection is provided by sensing the voltage drop across L801 against D808; this limits the maximum available drive to the base of the oscillator transistor, TR801, and hence its maximum collector current to approximately 600mA. If this current is maintained the fuse, FS832, will blow.

Adjustment of the EHT is by R854 "Set EHT" mounted on the power supply printed circuit board.

The full output from the transformer secondary is taken to a six stage multiplier module to provide +14kV for the final anode of the crt.

4.24 CATHODE RAY TUBE AND ITS INPUTS

The OS3350 employs a conventional mesh p.d.a. tube with a high efficiency aluminized screen.

The interconnection diagram, Fig. 9, shows the necessary connections to the various electrodes.

THE GUN

An independent winding on the mains transformer drives the heater for the cathode. The beam current and hence the spot intensity is controlled by the differential potential between the grid and cathode. The −2kV potential is the direct stabilised output from the EHT oscillator. The grid potential is the sum grid supply from the EHT oscillator and the output potential of the bright-up amplifier to which the grid supply is referred.

The crt beam is brough to a clear, well focussed spot by varying the potentials applied to the focus and astigmatism electrodes. These signals are derived from R82 (focus) and R81 (astigmatism) mounted on the front panel, the latter being a screwdriver adjustment. The focus electrode is normally variable over the range −530V to −740V and the astigmatism from +120V to 0V.

THE DEFLECTION SYSTEM

The Y plates are connected to the output of the Y amplifier and the differential signal applied, deflects the beam in the vertical direction. The mean plate potential is normally +75V and the sensitivity is approx. 5.2V/cm.

Similarly, the X plates are connected to the X output amplifier and the differential signal deflects the beam in the horizontal direction. The mean X plate potential is normally +95V and the sensitivity is approx. 16.6V/cm.

The deflection plate shield, S1, screens the deflection plates from the other electrodes and is held at a potential of +65V obtained from the junction of R919 and R920 on the interconnect p.c.b.

The interplate shield, S2, screens the X plates from the Y plates and is held at a potential 15V more negative than the X mean plate potential, derived from the wiper of R381 on the Y output p.c.b.

Having passed through the deflection plate system the beam accelerates to the screen which is held at +16kV relative to cathode by an output from the EHT oscillator, striking the phosphor at high velocity to produce the necessary bright trace.

THE TRACE ROTATION COIL

A coil, L83, fitted round the neck of crt, inside the magnetic shield is used to align the trace with the horizontal graticule lines.

The current for this coil is taken from the front panel potentiometer, R83 through R849, on the power supply board.

4.25 SCALE ILLUMINATION

The external scale is illuminated by two lamps, ILP83 and ILP84.

The supply for these lamps is derived from the emitter-follower, TR836, on the power supply board; being set by the scale illumination potentiometer, R80, on the front panel.

Both the emitter-follower and the control potentiometer are supplied from the full-wave rectified signal taken from the transformer at the junction of diodes, D83 and D84.

4.26 THE BEAM FINDER

Operation of the TRACE LOCATE push button performs the following functions.

Firstly, R85 is connected in a series with the +190 volt line that feeds the X and Y plate amplifiers. This limits the swing to approximately 8cm in the X direction and 12cm in the Y. To further limit the scan in the Y direction to 6cm, the current in the output stage is reduced by switching R366 in series with the normal emitter resistor of the current source transistor, TR355.

The Bright-Up amplifier is biased by resistors, R973 from the −15V line and R993 from the switched +190V line. The values are so arranged that 2mA flows into the amplifier input from the negative supply, allowing normal operation of the INTENSITY control. When the TRACE LOCATE button is pressed this bias current is changed, due to the voltage across R993 falling to 70V, thereby increasing the negative bias to approximately 4mA which gives full bright-up to the display, overriding the setting of the INTENSITY control.

Maintenance

Section 5

5.1 GENERAL

The instrument is electrically protected by five fuses as follows:-

1. 1A 'Slo-blo– size 20mm (FS83 Pt.No.34790) for the 95-130V Supply ranges.
   500mA 'Slo-blo' size 30mm (FS83 Pt.No.33685) for the 190-260V Supply ranges.
2. 250mA size 20mm (FS831 Pt.No.32338) in +190V supply line and mounted on the Power Supply board.
3. 500mA size 20mm (FS832 Pt.No.32339) in the +20V line supplying the EHT Oscillator also mounted on the Power Supply board.
4. 1A size 20mm (FS833 Pt.No.52162) in the +15V line and mounted on the Power Supply board.
5. 1A size 20mm (FS834 Pt.No.52162) in the –15V line and mounted on the Power Supply board.

Access to the four latter fuses is by removal of the bottom cover.

The following sections give information allowing access to and removal of the various printed circuit boards and assemblies as may be found necessary, during fault finding procedures.

If, during fault finding, a component needs replacing, it should be cut from the printed circuit board as close as possible to the component, leaving the wires connected to the copper track and protruding through to the component side of the board. The new component should then be soldered into position by attaching it to these protruding wires. This protects the copper track from damage.

If a fault on a printed circuit board cannot be cleared, it is recommended that the instrument is returned to the manufacturer for repair, When faults have been cleared it is recommended that the calibration procedure is implemented to ensure that the instrument conforms to the specification.

5.2 ACCESS

Figures 13, 14, 15, 16, illustrate various views of the instrument showing access to the majority of preset components when the top and bottom covers have been removed. Each cover is retained in position by four latch fasteners. Each fastener is released by turning it one quarter of a turn clockwise or counter-clockwise.

The construction of the instrument has been arranged so that individual boards and assemblies can be checked and components changed without actually removing the assemblies from the main frame or disconnection of cable forms. In the case of the timebase unit this has been achieved by making it a plug-in assembly which can be removed and operated on an extension lead, PL91. This assembly is then still fully functional and access is provided to both sides of both printed circuit boards.

The following description details the method for removing the individual assemblies:-

5.2.1 ATTENUATOR AND PRE-AMPLIFIER ASSEMBLY

1. Each assembly is fitted with its own screening cover and it is only necessary to remove the cover from the unit requiring attention. The procedure is identical for both attenuator assemblies.
2. Having removed the screen, take out the shift control spindle by loosening the grub screws on the universal coupling, also remove the coupling.
3. Unsolder the three supply leads and four signal leads from the rear of the horizontal printed circuit board.
4. Remove the knob from the VOLTS/cm selector switch and its fixing nut, the lever switch knob and the fixing stud behind the front panel mounted between the BNC socket and the lever switch.
5. The unit can now be removed by lifting first from the rear to clear the shift control support bracket and pulling towards the rear of the instrument.
6. For fault finding, the unit may be operated out of the frame by extending the supply and signal leads. Providing that the signal leads are kept reasonably short the complete channel may be checked at frequencies approaching the full bandwidth.

5.2.2 BEAM SWITCH & DELAY LINE EQUALISER BOARD

1. Disconnect the signal leads from the rear of the board (Pins 43 and 44) and remove the seven fixing screws.
2. Release the Delay Line from its retaining clips.
3. The board may now be brought carefully to the upright position without unsoldering any further connections. This operation then gives access to both sides of the board.
4. If it is required to operate the board in this position, it is recommended that the output should be re-connected via extended leads.
5. Raising this board also gives access to the SHIFT control potentiometers, the x5 GAIN pull switch and the CH2 INVERT switch.

5.2.3 DELAY LINE

1. The Delay Line is mounted above the shield, by means of clips through the top of crt shield.

5.2.4 OUTPUT BOARD

1. Remove the two Y Plate leads and the S2 connection from the tube side pins.
2. Remove the board fixing screws and also the screws attaching the output transistor heat sink to the tube support assembly.
3. The board, together with the output transistors, may now be swung out of the frame on the connecting leads giving access to both sides of the board.
4. The output transistors can be changed without removing the board by taking out the fixing screw and lifting off the moulded clamp.

5.2.5 TIMEBASE UNIT

1. Remove the fixing screws from the Timebase section of the front panel and also slacken the two fixing screws attaching the rear of the unit to the cross bar (see Fig. 6).
2. Carefully draw the Timebase Unit through the front of the instrument, taking care not to catch any components on the front extrusion.
3. Check that the polarising keys are still correctly positioned in the multiway connectors.

4. Unplug the ribbon cable from the socket SKC on the TV Sync Board.
5. Undo the four screws on the Timebase board that held the two TV Logic board brackets.
6. Lift out the TV Logic board from between the two other boards.
7. The TV Logic board can be mounted, from one of its brackets, outside the timebase unit, and with the ribbon cable again connected to the TV Sync Board, the whole unit can be operated on the extension lead, PL91, with all boards accessible.

5.2.6 BRIGHT-UP AMP AND X AMP BOARD

1. Remove the two X plate leads from the crt.
2. Remove two screws holding heat sink to top support bar.
3. Withdraw the printed board backwards to clear the p.c. connector and then lift upwards. Full access is then given to both sides of the board.

5.2.7 POWER SUPPLY ASSEMBLY

The low voltage power supply unit is on a removable sub-chassis mounted in the rear of the instrument.

1. Remove the screws securing the moulded rear cover, and remove the cover.
2. Remove the remaining screws holding the unit on to the rear extrusion and the screws supporting the Interconnect support bar and the Delay/Beam Switch printed circuit.
3. Remove the four screws in the rear cross bar.
4. The unit may now be removed from the frame as shown in Fig. 13, to the distance provided by the loop in the cable form.
5. Access is now provided to the mains transformer and VOLTAGE SELECTOR switch, smoothing capacitors and series stabiliser transistors.

5.2.8 POWER SUPPLY PRINTED CIRCUIT BOARD

1. Remove the board fixing screws and the heat sink bracket screws.
2. The board will now lift into the vertical position on its cable form giving access to both sides.

5.2.9 INTERCONNECT BOARD

Access to this board may be obtained by removing a number of units as previously described, namely – Timebase Unit, Bright-Up Amplifier and Power Supply Assembly.

5.2.10 EHT UNIT

1. Remove the two screws at the top of the box, which pass through the box and into the centre bar of the instrument.
2. Lift the box out of the instrument on its cable form.
3. Remove the six screws which hold the lid and remove. Insert one of the long fixing screws through its original hole in the rear of the box and screw into the threaded insert provided in the centre bar of the instrument. This secures the unit for servicing purposes.
4. The oscillator printed circuit board and transformer are now accessible. The printed circuit board may be removed by unsoldering leads to multiplier and TR801 and then four fixing screws.

5.2.11 CATHODE RAY TUBE

1. Access to the base of the tube is possible by removing the moulded cover which is attached to the rear of the instrument.
2. The tube may be removed by withdrawing from the front after taking off the escutcheon and filter assembly.
3. Before attempting to extract the tube, remove the side pin connectors and the base. It will also be necessary to unsolder the twist coil leads from the interconnection printed circuit board (pins TWIST and 0V). The twist coil is attached to the tube and therefore its leads should be fed through the hole in the shield as the tube is pulled out.
4. Care should be taken when removing the tube not to bend the side pins as this may crack the glass around the seal.

5.3 FAULT FINDING TABLES

Faults may be localised by reference to the Fault Localisation information presented on pages 48 to 42 and the Circuit Voltages listed in Section 5.4 which should be used as a general guide of voltage obtainable at certain locations within the instrument and can be used as an aid to servicing.

The power supply input voltage should be approximately at the mid range of the Supply Voltage setting. The power supply voltages in the tables are those appearing under these conditions. Other voltages assume that the Y inputs are grounded and the amplifiers are set to 5mV/cm sensitivity. The Timebase is set to FREE RUN, CH1 mode with CH1 trace brought to the centre of the screen.

5.4 OPERATING POTENTIALS

(a) INPUT ATTENUATOR AND PRE-AMPLIFIER

Location		Voltage
TR102	Drain	approx. 0V
TR103 and TR104	Collectors	13.5V
TR103 and TR104	Emitters	+0.7 to +2.7V
TR121 and TR122	Collectors	+4V
TR120	Collector	−5.5V
TR123 and TR124	Collectors	+6.6V
TR125 and TR126	Bases	+8.6V
"Trig" output		+7.9V
"Sig" output		+7.6V

(b) BEAM SWITCH AND DELAY LINE EQUALISATION

Location		Voltage
TR201, 202, 207 and 208	Emitters	+8.6V
TR202, 208 and 220	Collectors	Nominally 0V
TR207	Collector	+0.8V
TR203, 204, 205 and 206	Collectors	+5.4V
TR209	Collector	+2.5V

TR209	Base	+0.8V
Y2 O/P		Nominally 0V
TR210 and TR211	Collectors	+6.3V
TR214	Collector	+7.4V
Pin 31 and 33		+5V
TR215	Collector (CH1 Selected)	+2V
TR215	Collector (CH2 Selected)	+7V
TR217	Collector	+13.7V
TR218	Collector	+2.8V
TR219 and TR220	Emitters	+6.8V
TR300 and TR301	Emitters	+4.1V
TR300 and TR301	Collectors	−1.4V
TR302 and TR303	Collectors	−2.3V
TR304 and TR305	Collectors	+3.8V
Pins 43 and 44		+2.4V

5.5 CALIBRATION PROCEDURE

5.5.1 TEST EQUIPMENT

1. Variable autotransformer. Output voltage 95 to 260V at 1A with ac rms voltmeter (Variac).
2. Digital Multimeter with 10MΩ input impedance, 4½ digit, accuracy within 0.1%.
3. High voltage probe for Digital Multimeter capable of operating up to 20kV.
4. Time Mark Generator. Marker generator of 0.1µs to 1 sec, accuracy within 1%.
5. Squarewave Generator. 1MHz flat top square wave generator with adjustable amplitude 0.1V to 1V into 50 ohms having a rise time of less than 2ns.
6. RF Sinewave Generator. 500kHz to 60MHz with 50kHz reference frequency. Output amplitude 25mV to 5V p-p into 50 ohms. Amplitude accuracy at 50kHz and 500kHz to 60MHz within 2%.
7. LF Sinewave Generator.
8. Capacitance Standardiser. 1MΩ/28pF, BNC 50Ω termination. BNC - BNC connector leads (PL43 & PL94). Timebase Extension Lead PL91. Video Z mod/Picture drive link (PL106).
9. Colour Calibrator. 3.58MHz subcarrier switched at 10kHz.
10. OFF-AIR VIDEO SOURCE (nominally 1V p-p video + sync) into 75Ω.
11. DUAL BEAM OSCILLOSCOPE (preferably with TV trigger). Sensitivity 5mV/cm: Bandwidth 10MHz.
12. Stable dc voltage source capable of supplying 50mA at 2V.

NOTE: Calibration should be carried out at normal ambient temperature and should not be commenced until the instrument has been operating for at least 15 mins.

5.5.2 SET SUPPLY RAIL VOLTAGE

1. Set the INTEN control to minimum.
2. Set the SUPPLY VOLTAGE switch on the rear panel to suit the supply. Apply the supply voltage via the Variac set to mid-range of the Supply Voltage setting.
3. Check that the SCALE control varies the scale intensity and that the neon, N80, is energized
4. Connect the digital meter between chassis and pin '−15V' on the Power Supply printed circuit board. Adjust the voltage to −15V ±2% by means of R838.
5. Check that the voltage to chassis on the following pins on the Power Supply printed circuit board, are within the following limits:

'+15V'	+15	±4%
+190V	+190V	±4%

6. Connect a HV probe to the meter to read 2500V, and meter between chassis and pin 'VK' on Bright-Up Amplifier printed circuit board. Adjust R854 on Power Supply printed circuit board for a reading of −2000.
7. Check that EHT supply at tube cavity cap connector is 14kV ± .7kV.

5.5.3 SET TUBE CUT-OFF AND VISIBLE DELAY

Due to small changes in the crt control grid characteristics during warming up, the first part of the adjustment should be made as soon as a trace appears after switch-on.

Advance BRIGHTNESS control to the '9 o'clock' position. Adjust R988 on Bright-Up Amplifier printed circuit board so that the trace is just not visible.

Set the TIMEBASE controls such that the oscilloscope functions with CH1 or CH2 trigger and in the normal (i.e. not TV) mode. Set the Range switch to give a sweep rate of 20ns/cm. Inject the 1MHz fast rise pulse and adjust the trigger so that the leading edge is visible.

5.5.4 Z MODULATION

1. Apply a 1kHz square wave of 5V amplitude to the Z MOD socket on the rear panel and to CH1 INPUT socket with CH1 VOLTS/cm switch set to 2V.
2. Obtain a stable trace and check that the modulation is just visible.
3. Increase input to 20V p-p, check that the trace can be fully blanked and that positive signals cut off and negative signals bright up the trace.

5.5.5 ADJUST TRACE ALIGNMENT

Set Timebase to 1ms/cm and TRIGGER SELECT to FREE RUN.

Adjust R850 (Trace rotation preset) to bring the trace parallel to the horizontal center line.

5.5.6 GEOMETRY

Apply to CH1 INPUT a 1kHz sinewave to give an amplitude of 8cm, adjust ASTIG and FOCUS controls for a sharp display and set Timebase to display approximately 10 cycles. Adjust R381 (on the Y O/P board) for a comromise between horizontal and vertical deflection to eliminate pincushion and barrel distortion. Reset ASTIG and FOCUS controls if necessary.

5.5.7 X AMPLIFIER ADJUSTMENTS

These adjustments should be carried out with the TB unit on an extension lead, PL91, to give access to controls.

1. Set TIME/cm to EXT X and VARI TIME/cm control to CALIBRATED. Also set the DISPLAY SELECT switch to either CLAMP or CLAMP OUT.

2. Inject a 10V p-p 1kHz square wave into the EXT X socket.
3. Adjust R935 on X amplifier and Bright-Up printed circuit board, to give 10cm of X deflection.
4. Pull the Fine X Shift (x5 Amp gain).
5. Inject a 2V p-p 1kHz square wave into the EXT X socket.
6. Adjust R936 on X amplifier and Bright-Up printed circuit board, to give 10cm of X deflection. Switch back to x1 amp gain.
7. Inject an 8V p-p 10kHz square wave into the EXT X socket. Adjust C684 (on TV logic printed circuit board) to remove any 'tail' which extends beyond the bright spots at the extremes of the deflection.

5.5.8 TIMEBASE ACCURACY ADJUSTMENT

These adjustments should be carried out with the Timebase operating on an extension lead, PL91, to give access to the appropriate controls.

Timebase:

1. Set TIME/cm to 1ms/cm, VARIABLE TIME/cm control to CALIBRATED.
2. Inject 1kHz marker pulses into CH1 channel and trigger for stable trace.
3. Adjust R510 on the Timebase printed circuit board for 1 marker pulse per cm.
4. Set the Timebase Range Switch to 0.1µs/cm, VARIABLE TIME/cm control to CALIBRATED.
5. Inject 10MHz marker pulses into CH1 channel and trigger for a stable trace.
6. Adjust C435 on the Timebase printed circuit board for 1 marker pulse per cm.
7. Check that TIME/cm VARIABLE gives greater than 3:1 reduction in speed.

5.5.9 TRIGGER LEVEL SLOPE BALANCE ADJUSTMENT

Adjustment to be carried out with Timebase on extension lead PL91.

1. Inject a 1kHz sine wave into CH1 and set TRIGGER LEVEL control to mid-position, Trigger Coupling in AC/TV position.
2. Adjust R453 ("slope Bal") so that there is no significant movement of the trigger point when the TRIGGER SELECT switch is moved from "+ve to −ve".
3. Move TRIGGER COUPLING to dc position and adjust R213 to obtain the same trigger point. Repeat using CH2 channel and R223.

NOTE: R213 and R223 are situated on the Delay Drive/Beam Switch printed circuit board assembly.

5.5.10 CHANNEL 1 & 2 FINE GAIN CONTROL BALANCE

1. Set CH1 VOLTS/cm switch to 5mV, INPUT COUPLING switch to GND, Mode switch to CH1, Timebase to Free Run.
2. Set trace on centre line by means of CH1 shift control. Adjust front panel BAL control to give no trace movement when the CH1 FINE GAIN control is operated.
3. Repeat procedure for Channel 2.

5.5.11 CHANNEL 1 & 2 STEP ATTENUATOR BALANCE

1. Set CH1 VOLTS/cm switch to 20mV, INPUT COUPLING switch to GND, Mode switch to CH1, Timebase to Free Run.
2. Set trace on centre line by means of CH1 SHIFT CONTROL. Adjust Step Bal (CH1) to give no trace movement when the VOLT/cm switch is moved to 5mV/cm.
3. Repeat procedure for Channel 2, adjusting Step Bal (CH2).

5.5.12 X5 GAIN BALANCE/INVER BAL (CH2)

1. Set CH1 VOLTS/cm switch to 5mV INPUT COUPLING switch to GND, Mode switch to ~~Y1,~~ CH1 12-12-90 BC Timebase to Free Run.
2. Set trace on centre scale line by means of CH1 shift control. Adjust R146 (CH1) so that no trace shift occurs when the X5 pull switch is operated.

5.5.13 DELAY LINE MATCHING

1. Set CH1 VOLTS/cm switch to 20mV, inject 1MHz square wave to give 6cm deflection, adjust trigger to give stable trace.
2. Inspect top of waveform for any step occurring approximately 200~~µs~~ ns after the start of the pulse. 12-12-90 BC
3. If any step is present replace A.O.T. resistor, R625, with a small 220Ω carbon potentiometer on short leads, adjust for no step, measure required value and substitute fixed resistors of nearest preferred value.

5.5.14 'ADD MODE' AMPLIFIER BALANCE

1. Set FUNCTION SWITCH to CHOP and bring both traces to the centre horizontal line, by means of CH1 and CH2 SHIFT controls.
2. Set the MODE SWITCH to ADD and note the direction and amount of movement of the trace. Return to CHOP Mode.
3. Add 100kΩ potentiometer across A.O.T. position, R294 or R295, to give a direction of movement the same as that given when moving from CHOP to ADD.
4. Adjust potentiometer to bring both traces to position found in '2'.
5. Re-centre traces, switch to ADD, movement should now be less than 0.5cm.
6. Replace potentiometer with fixed resistor of the nearest preferred value.

5.5.15 CHANNEL 1 and 2 GAIN ADJUSTMENT

1. Set CH1 VOLTS/cm switch to 20mV, INPUT COUPLING switch to dc. FINE GAIN CONTROL to Cal.
2. Inject a 1kHz square wave having an amplitude of 120mV into CH1, adjust R227 (Set Gain CH1) to a deflection of 6cms.
3. Switch to 10mV range, inject 60mV and adjust R138 (CH1) to give 6cm deflection.
4. Switch to 5mV range, inject 30mV and adjust

R136 (CH1) to give 6cm deflection.

5. While still on 5mV range, inject 6mV, pull for X5 gain and adjust R229 to give 6cm deflection.
6. Switch to all other ranges and inject the appropriate signal to give 6cm deflection. Check that all ranges are accurate to within ±3%.
7. Repeat the above procedure for Channel 2, the adjustments for the 20mV, 10mV, 5mV and 1mV ranges being respectively, R231, (Set Gain CH2), R138 (CH2) and R136 (CH2). (X5 gain not applicable.)

5.5.16 CHANNEL 1 and 2 ATTENUATOR COMPENSATION

1. Ensure that the attenuator covers are correctly fitted and that the link across the universal coupling on the SHIFT control is continuous.
2. Set CH1 VOLTS/cm switch to 20mV, INPUT COUPLING switch to dc. Inject 200mV 1kHz square wave via the 28pF/1MΩ standardizer Trigger for stable trace.
3. Adjust input trimmer, C171 (CH1), for square corner.
4. Remove standardizer switch VOLTS/cm to 0.2V, inject 1V square wave and adjust X10 compensating trimmer, C167 (CH1), for square corner.
5. Inject 2V square wave via standardiser and adjust X10 input trimmer, C165 (CH1), for square corner.
6. Remove standardizer, switch VOLTS/cm to 2V, inject 10V square wave and adjust X100 compensating trimmer, C161 (CH1), for square corner.
7. Inject 20V square wave via standardizer and adjust C100 input trimmer, C159 (CH1), for square corner.
8. Remove standardiser and check all attenuator ranges, applying the appropriate amplitude, to ensure all ranges give a square corner to the applied waveform and are accurate to within ±3%.
9. Repeat above for Channel 2, the component numbering is the same except for a suffix 'CH2'.

5.5.17 Y2 OUTPUT AMPLITUDE AND PHASE ADJUSTMENT

1. Set CH1 and CH2 INPUT VOLTS/cm switches to 0.1V. INPUT-COUPLING switches to dc. Link CH2 OUTPUT to CH1 INPUT. FUNCTION SWITCH to ALT. FINE GAIN CONTROL to CAL.
2. Inject 0.5V 1kHz square wave into CH2 input, trigger for a stable trace.
3. Adjust R238 to give equal deflections on CH1 and CH2 (i.e. CH2 Output of 100mV/cm).
4. Remove CH2 OUTPUT link from CH1 INPUT and take to EXT X and PULL X5. (TIME C/M Sw.)
5. Apply a sine wave source to CH1 and CH2. Adjust input level to give a convenient size display which should be a 45° line at low frequencies.
6. With input frequency of 500kHz, adjust capacity (approx. 15pF) C228 (A.O.T.) until ellipse just closes. (Max. phase shift 3°, dc – 500kHz.)

5.5.18 Y AMPLIFIER OVERALL PULSE RESPONSE

1. Set CH1 and CH2 VOLTS/cm switch to 20mV, INPUT COUPLING switch to dc. Ensure that the A.O.T., R230 and R235, are initially not in circuit. FINE GAIN CONTROLS to CAL.
2. Select CH1 mode and inject 100mV square wave at 100kHz. Adjust R309 to give optimum flat top response.
3. Change input frequency to 1MHz. Adjust R311 to give a response having approximately 20% undershoot over the first 35–40ns.
4. Adjust C311 to improve the edge response without affecting adjustment 3.
5. Adjust C322, R357 and C357 for optimum leading edge and corner with no overshoot or hook.
6. Connect a small carbon 1kΩ potentiometer on short leads across A.O.T. pins R230. Adjust potentiometer and C202 to remove undershoot left in adjustment 4 and 5. Replace potentiometer with fixed resistor.
7. Inject 1MHz signal into CH2 and repeat adjustment 6 to establish correct value of R235.
8. Adjust C211 to give improvement in, without increasing, overshoot over first 15μs.

5.5.19 5mV and 10mV HF COMPENSATION

1. Set CH1 and CH2 VOLTS/cm switch to 10mV, INPUT COUPLING switch to dc, FINE GAIN CONTROL to CAL.
2. Select CH1 mode and inject 50mV square wave at 1MHz. Adjust C123 (CH1) to give a square corner.
3. Switch to 5mV/cm, inject 25mV and adjust C122 (CH1) to give a square corner.
4. Repeat 2 and 3 for CH2 input, adjusting C123 (CH2) and C122 (CH1) respectively.

5.5.20 BANDWIDTH

1. Set CH1 and CH2 VOLTS/cm switches to 20mV, INPUT COUPLING switch to dc. FINE GAIN CONTROL to CAL.
2. Select CH1 mode and inject 50kHz from Constant Amplitude Generator to give 5cm deflection. Increase the frequency of the generator until the display amplitude falls to 3.5cms. The frequency should be greater than 40MHz.
3. Repeat '2' for 10mV and 5mV positions on CH1 and for 20, 10 and 5mV positions on CH2.
4. Repeat to 1mV/cm (X5 gain) on CH1 where the bandwidth should be greater than 10MHz.

5.5.21 CHOP WAVEFORM COMPENSATION

1. If any of the transistors or diodes associated with the beam switch are changed it may be necessary to readjust the capacitive balance of the circuit.
2. Set INPUT COUPLING switch to GND. Couple EXT TRIG via probe to the collector of TR218 (R283). Turn TRIG SELECT to EXT.
3. Switch to CHOP mode and set the two traces 0.5cm either side of the centre line by means of the SHIFT controls and adjust the Timebase

(1μs/cm) so that individual chop transitions are visible.

4. Small amounts of capacity should be added between points 26 and 25 or 26 and 27 for CH1, and between 29 and 28 or 28 and 30 for CH2, to ensure that the chop transitions are flat and parallel to the center line. The capacity required is usually small and is most easily achieved by using short lengths of enamelled copper wire twisted together.

TIMEBASE WAVEFORMS

These are drawn for the following conditions. The timebase is switched to 0.1ms/cm and a 5cm 10kHz square wave is applied to the CH1 channel. The trigger is set to CH1 +ve slope.

The video measurements are carried out with a 1V p-p video signal input into 75 ohms, and with the video attenuator set to the 1V range. Normally the instrument is set to display the CLAMP mode, except for the line and field ramp waveforms where PICTURE mode should be selected.

TV ADJUSTMENTS

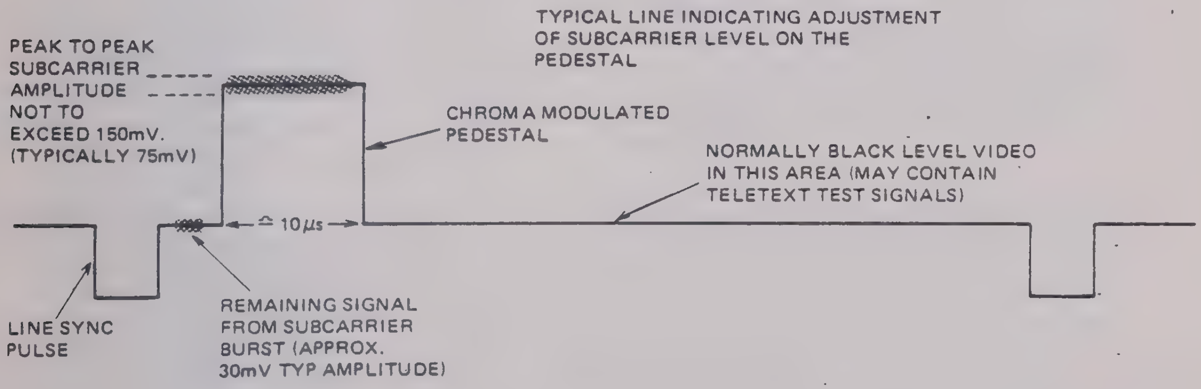
Adjustments to be carried out with the timebase connected on an extension lead, PL91.

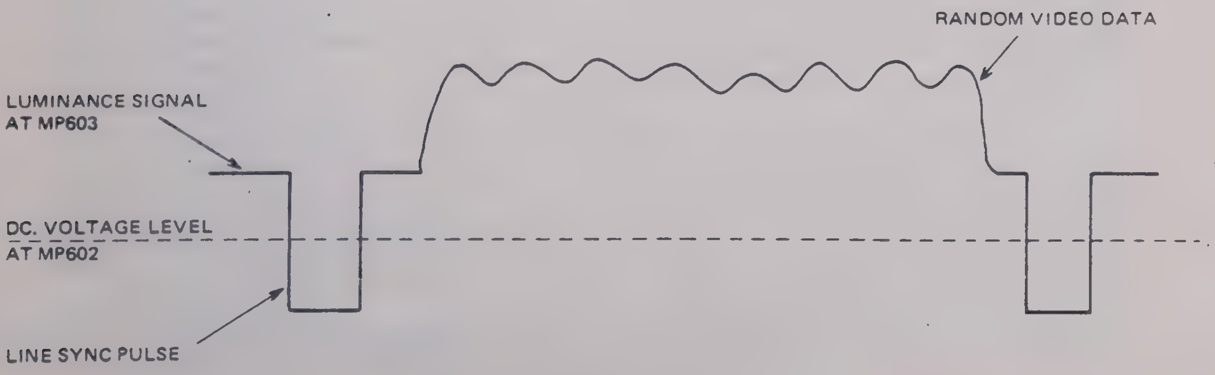
5.5.22 SUBCARRIER TRAP

1. Set the video attenuator to 1V range and the DISPLAY switch to CLAMP OUT. Connect a 1V p-p off-air video source to the video in socket.
2. Connect a X10 probe from the CH2 input on the main frame to TR610 emitter on the monitor point. MP616.
3. Switch the CH2 attenuator to 20mV/cm with input coupling set to ac.
4. Set the VIDEO SELECT switch to trigger on a line containing a chroma modulated pedestal as an insertion test signal. (If TV trigger is not yet functional use a test oscilloscope with TV trigger facilities for this test.)
5. Adjust for minimum 3.58MHz subcarrier on the pedestal. Check that the amplitude is less than 150mV.

5.5.23 SYNC SEPARATOR SLICING LEVEL

1. Set both channels of the test oscilloscope to 20mV and the input switches to dc. Using a X10 probe on each channel input, connect both probes to test point, MP602.
2. Position both traces on the centre horizontal graticule line, then transfer one probe to MP603.
3. Check that the dc signal lies between 45 to 55% of the sync pulse amplitude. If necessary change R674 to achieve this.


TYPICAL LINE INDICATING ADJUSTMENT OF SUBCARRIER LEVEL ON THE PEDESTAL
PEAK TO PEAK SUBCARRIER AMPLITUDE NOT TO EXCEED 150mV. (TYPICALLY 75mV)
CHROMA MODULATED PEDESTAL
NORMALLY BLACK LEVEL VIDEO IN THIS AREA (MAY CONTAIN TELETEXT TEST SIGNALS)
≏ 10μs
LINE SYNC PULSE
REMAINING SIGNAL FROM SUBCARRIER BURST (APPROX. 30mV TYP AMPLITUDE)


RANDOM VIDEO DATA
LUMINANCE SIGNAL AT MP603
DC. VOLTAGE LEVEL AT MP602
LINE SYNC PULSE

5.5.24 DELAY RANGE

1. Connect the VIDEO OUT to the main frame CH2 input. Set the attenuator to 50mV/cm and the input coupling to dc.
2. Set the TRIGGER SELECT switch to TV and the trigger coupling to ac TV. Set the DISPLAY switch to CLAMP OUT.
3. Select a suitable line (e.g. line 17, field 1) on the VIDEO SELECT switch and check that adjustment of the trigger level control produces a steady triggered video display (not a bright display). Triggering should be stable over approx. 90° of the control range.
4. Check that the DELAY control enables the trigger point to be varied over a range of 90μs ± 10μs.
5. Set TRIGGER SELECT switch to OVERLAY and check that a trace with a fixed trigger point before the leading edge of line sync is superimposed on the delayed trace identified above.

5.5.25 VIDEO SELECT FUNCTIONS

Set TRIGGER SELECT switch to TV. Check that the TV trigger functions operate correctly for the following modes:

1. FIELD	Trigger point should be just after the first broad pulse. With the FIELD SELECT switch in field 1 position, the trigger point should be roughly in the middle of line 4 field 1. In the field 2 position, it should be just before line 4, field 2. In the both fields position, both fields are displayed superimposed.
2. LINE REP	Triggering occurs on alternate lines and should produce a bright display.
3. LINE SELECTOR	Check that the LED display comes on only in this mode. Press the LINE SELECT switch "UP" and check that the count increases slowly for the first four counts and then counts more rapidly. Check that the count goes from line 001 to 263 and then on to 001 again. Press the switch "DOWN" and check that the count decreases in a similar manner. Select line 4, field 1, and check that trigger occurs prior to to first broad pulse of line 1. Select field 2, check that the line count does not change, and check that trigger is before the second broad pulse of line 4. Select both fields and check that the broad pulses of both fields are superimposed.
4. LINES 15–21	Select each line on the VIDEO SELECT switch, individually, and identify them on the TV waveform. This can be done by counting back from a indentifiable line on the waveform, or by inspecting the picture and comparing it with the same line viewed in the LINE SELECTOR mode.

5.5.26 PICTURE

1. Connect the link (PL106) between the rear panel sockets, PICTURE DRIVE and Z MOD.
2. With the off-air signal still connected, switch the DISPLAY SELECT switch to PICTURE.
3. A 525 line picture should now appear on the screen. Set the VIDEO SELECT switch to the LINE SELECTOR position and set the count display to read about 150.
4. As the DELAY CONTROL is advanced an intensified line should appear about half way down the raster. With the DELAY control set to maximum, the bright line should cover completely one line, starting about 1cm from the end of the line above it and finishing about 1cm after the start of the line below it.
5. Reduce the DELAY control to minimum and the intensified line should reduce to a small dot just before the end of one line. Increase the DELAY to MAX again.
6. Advance the counter by pressing the LINE SELECT switch 'UP'. Check that the intensified line moves down the raster. Then press the LINE SELECT switch 'DOWN' and check that the line moves up the screen.

5.5.27 PICTURE SIZE

1. Check that the picture height is 6.5cms (± 10%), 6cms of main picture + about 0.5cm of pre-picture data.
2. The picture width should be 8cms (± 10%). If not adjust the value of R759 (A.O.T.) to achieve this.

5.5.28 SUBCARRIER TRAP

1. Switch the DISPLAY switch to CLAMP.
2. Connect a X10 probe from the test oscilloscope to monitor point MP605. Adjust C606 for minimum color burst during the back porch clamp pulse period. If C606 has insufficient range change the A.O.T. component, C607, to 330pF or 390pF.

5.5.29 DC LEVEL

1. Disconnect the video input signal.
2. Connect the digital multimeter on a 100mV range to MP604. Set the potentiometer, R617, for 0V ±5mV.
3. Connect the VIDEO OUT to CH2 input. Set the CH2 input to GND and the attenuator to 10mV/cm. Then center the trace on the crt.
4. With the DISPLAY switch still in the CLAMP position check that not more than ±20mV of offset

between GND and dc input coupling positions. If necessary change the value of R625 (A.O.T.) to achieve this.

5. Now adjust R617 for no movement on the trace when the CH2 input is switched between GND and dc (within ±5mV).
6. With the trace centered on the middle line of the graticule and the input of CH2 set to dc, connect the off-air video signal to the VIDEO IN socket. Black level occurring during the Back Porch should be maintained at 0V ±5mV.

5.5.30 CALIBRATOR ADJUSTMENT

1. Disconnect the leads connecting to the VIDEO IN and VIDEO OUT sockets. Now connect a digital multimeter on the 1V range across the centre pin and chassis earth of the VIDEO OUT socket.
2. Now it is necessary to stop the calibrator oscillating by connecting a shorting link between TR644 emitter and chassis earth. (This is conveniently done by connecting to the appropriate end of R783 and the timebase main chassis.)
3. With the 'CAL' front panel button pressed adjust the potentiometer, R786, for 250.0mV on the DMM, and then release the button.
4. Now reconnect the DMM input to the 1V calibrator output pin on the front panel. Check that this reads 1V ±1%. The shorting link on TR644 emitter should now be removed.
5. Reconnect the off-air signal to the VIDEO IN and the link from VIDEO OUT to CH2. Set CH2 to 50mV/cm and dc coupling. Set the timebase range to 1ms/cm and the trigger to CH2 +ve and AUTO-level.
6. When the CAL push button is pressed the video signal should be interrupted and a 5cm square wave signal (±3%) should appear on the crt. Then adjust the calibrator frequency by R781 so that 1 cycle/cm appears against the graticule markings. (The calibrator frequency should be 1kHz ±5%.)

5.5.31 INPUT IMPEDANCE

1. Disconnect the off-air video signal from the VIDEO IN socket and connect the digital multimeter on the 100Ω range between the centre pin of the socket and chassis ground.
2. Check that the input impedance is maintained at 75Ω ±1% over all three ranges of the attenuator 0.5V, 1V and 2V.

VIDEO ATTENUATOR CALIBRATION

1. Switch the DISPLAY switch to CLAMP OUT and remove the link connecting the VIDEO OUT to CH2 input.
2. Connect a dc supply source of voltage set to about 1V to the VIDEO IN socket center pin and the 0V to chassis earth.
3. Connect the DMM on the 1V range across the VIDEO OUT socket. Set the video attenuator on the 1V range and adjust the dc supply for a reading of 250.0mV on the DMM.
4. Now switch to the 2V video attenuator range and check that the reading is 125mV ±0.5%.
5. Finally switch to the 0.5V range and check for a DMM reading of 500mV ±0.5%.

5.5.32 CLAMP OUT CALIBRATION

1. Connect the VIDEO OUT to CH2 input link. The DISPLAY switch should be set to CLAMP OUT.
2. Set CH2 input to dc 20mV/cm. The timebase range switch should be set to 0.5ms/cm and the trigger to CH2 +ve with AUTO level.
3. Press the CAL button and adjust the CH2 variable gain control for exactly 8cms display. This control setting should now be left for the next stage.
4. Connect the 10kHz 1V square wave output from the colour calibrator to the VIDEO IN socket. With the video attenuator on the 1V range check for 8cms vertical deflection on the crt to be within ±1% (±0.8mm).
5. Now switch the colour calibrator to give 10kHz + 3.58MHz output (500mV @ 10kHz, +500mV @ 3.58MHz). Set CH2 attenuator to 20mV/cm with the variable gain to the CAL position. Set the TRIGGER SELECT to the FREE RUN position.
6. The 10kHz modulated subcarrier will produce a continuous untriggered display on the screen. By observing the mid point of the signal and operating the ±0.1dB switch (which adjusts the amplitude of the subcarrier) check that the subcarrier is made to overlap or open out by equal amounts. If the movement of the subcarrier is not symmetrical adjust A.O.T., C611, on the video attenuator until this condition can be achieved.

5.5.33 CLAMP GAIN CALIBRATION

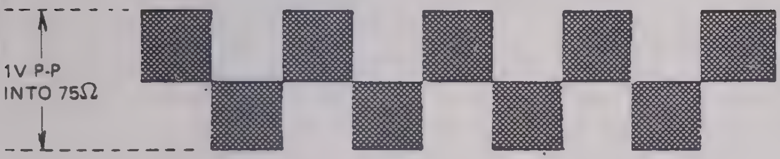
1. Set the DISPLAY switch to CLAMP. CH2 input to 20mV/cm. Set the TRIGGER SELECT switch to CH2 +ve and trigger to AUTO.
2. Remove IC600 (CD4098) from its socket to disable the clamp.
   NB. It is preferable to switch the instrument off while performing this operation to avoid damage to the circuitry.
3. Press the CAL button and adjust the variable CH2 gain control for exactly 8cms display. With the video attenuator set to the 1V position connect the 1V @ 10kHz input from the color calibrator and check that the display amplitude is 8cms within less than ±1%. If necessary select a value for R628 which gives the closest match to 8cms.

(Note: IC600 must be removed to disable clamp and prevent distortion on high negative signal amplitude.)

4. Replace IC600.
5. Switch the DISPLAY switch to CLAMP OUT and check for agreement of 8cms display amplitude

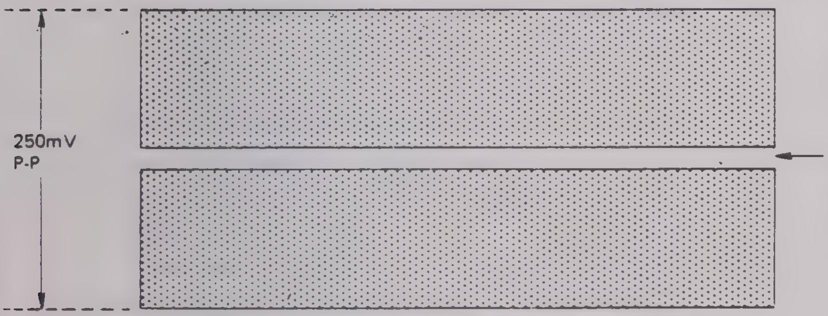
within ±1% of the CLAMP amplitude. If not reselect the value of R628 to achieve this limit and that of stage 3.

6. Switch the DISPLAY switch to CLAMP. Set the color calibrator to give a 500mV modulated 10kHz + subcarrier and adjust C605 (A.O.T.) to give equal overlap of subcarrier by a similar manner to that employed in the CLAMP OUT calibration previously described (stages 5 and 6).



3.58MHz SUBCARRIER MODULATED BY 10kHz SQUARE WAVE.

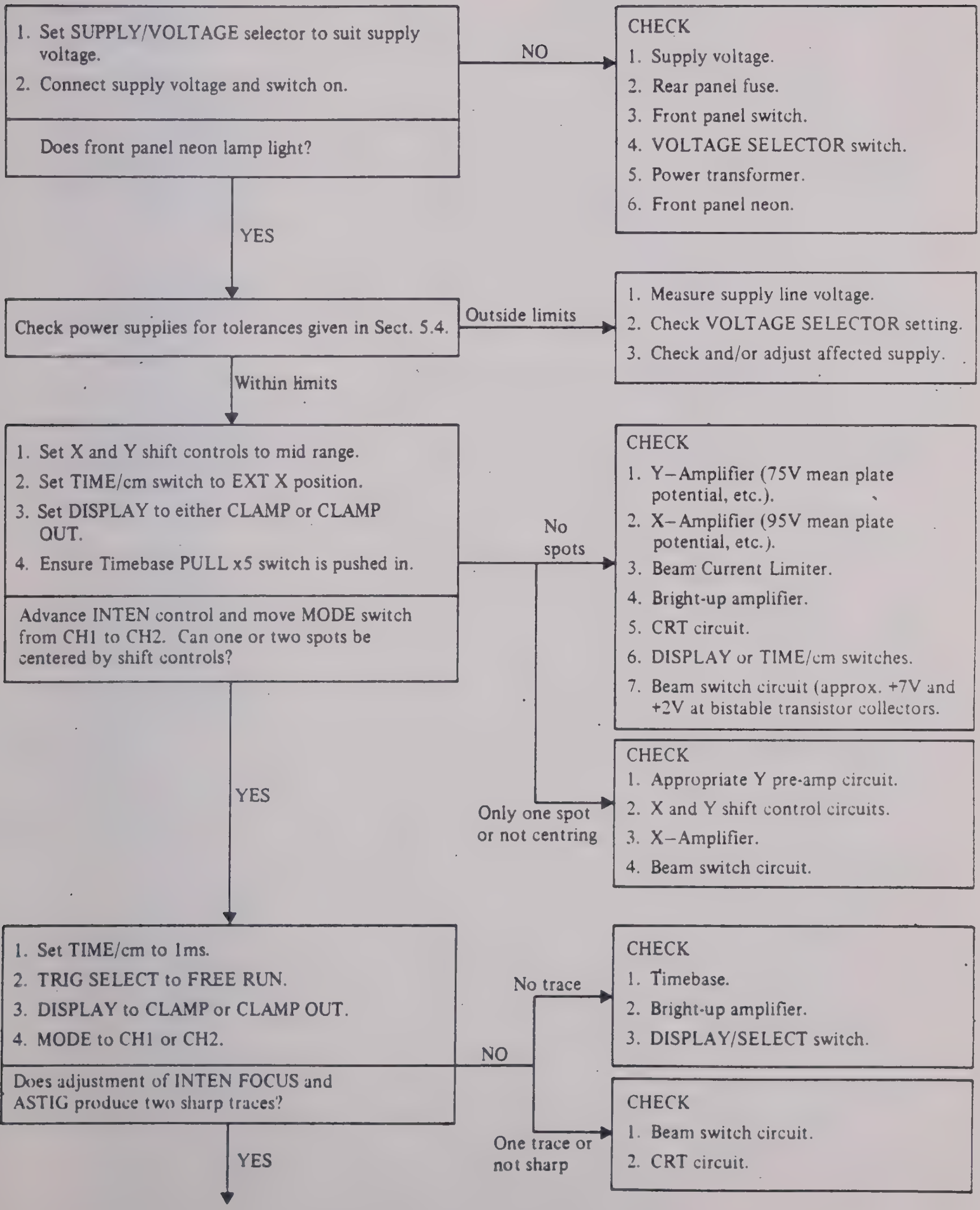
OUTPUT FROM COLOR CALIBRATOR.



THE SAME SIGNAL VIEWED AT THE OUTPUT FROM VIDEO OUT SOCKET WITH TIMEBASE ON FREE RUN.

ALIGN C611 TO GIVE EQUAL GAP/OVERLAP OF SUBCARRIER BY ADJUSTMENT OF ± 0.1dB SWITCH. AT CAL POSITION SUBCARRIER TRACES SHOULD JUST MERGE.

FAULT LOCALIZATION CHART



1. Set SUPPLY/VOLTAGE selector to suit supply voltage.
2. Connect supply voltage and switch on.

Does front panel neon lamp light?

CHECK
1. Supply voltage.
2. Rear panel fuse.
3. Front panel switch.
4. VOLTAGE SELECTOR switch.
5. Power transformer.
6. Front panel neon.

Check power supplies for tolerances given in Sect. 5.4.

1. Measure supply line voltage.
2. Check VOLTAGE SELECTOR setting.
3. Check and/or adjust affected supply.

1. Set X and Y shift controls to mid range.
2. Set TIME/cm switch to EXT X position.
3. Set DISPLAY to either CLAMP or CLAMP OUT.
4. Ensure Timebase PULL x5 switch is pushed in.

Advance INTEN control and move MODE switch from CH1 to CH2. Can one or two spots be centered by shift controls?

CHECK
1. Y–Amplifier (75V mean plate potential, etc.).
2. X–Amplifier (95V mean plate potential, etc.).
3. Beam Current Limiter.
4. Bright-up amplifier.
5. CRT circuit.
6. DISPLAY or TIME/cm switches.
7. Beam switch circuit (approx. +7V and +2V at bistable transistor collectors.

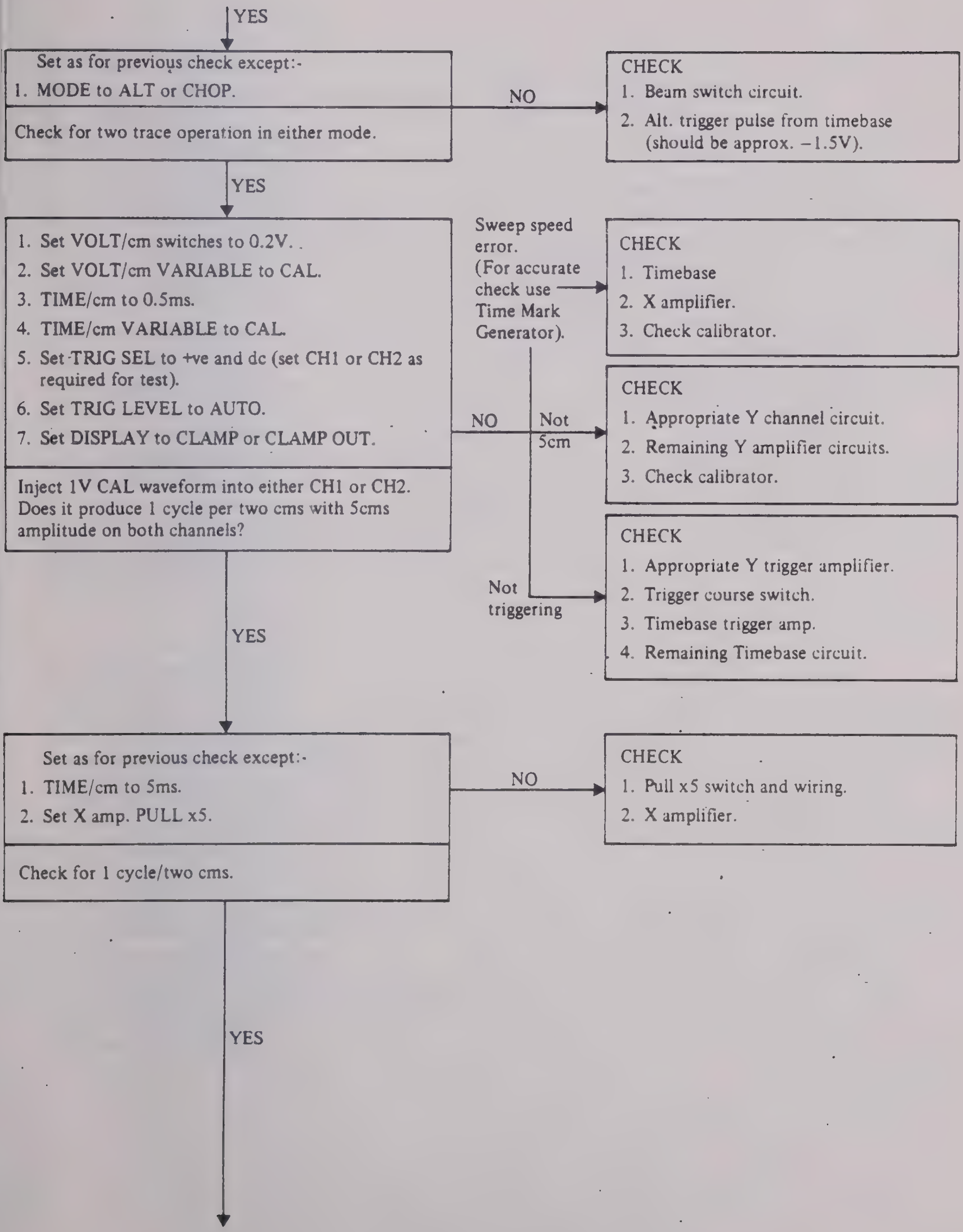
CHECK
1. Appropriate Y pre-amp circuit.
2. X and Y shift control circuits.
3. X–Amplifier.
4. Beam switch circuit.

1. Set TIME/cm to 1ms.
2. TRIG SELECT to FREE RUN.
3. DISPLAY to CLAMP or CLAMP OUT.
4. MODE to CH1 or CH2.

Does adjustment of INTEN FOCUS and ASTIG produce two sharp traces?

CHECK
1. Timebase.
2. Bright-up amplifier.
3. DISPLAY/SELECT switch.

CHECK
1. Beam switch circuit.
2. CRT circuit.



YES
NO
YES
Sweep speed error. (For accurate check use Time Mark Generator).
NO
Not 5cm
Not triggering
YES
NO
YES

Set as for previous check except:-
1. MODE to ALT or CHOP.

Check for two trace operation in either mode.

CHECK
1. Beam switch circuit.
2. Alt. trigger pulse from timebase (should be approx. −1.5V).

1. Set VOLT/cm switches to 0.2V.
2. Set VOLT/cm VARIABLE to CAL.
3. TIME/cm to 0.5ms.
4. TIME/cm VARIABLE to CAL.
5. Set TRIG SEL to +ve and dc (set CH1 or CH2 as required for test).
6. Set TRIG LEVEL to AUTO.
7. Set DISPLAY to CLAMP or CLAMP OUT.

Inject 1V CAL waveform into either CH1 or CH2. Does it produce 1 cycle per two cms with 5cms amplitude on both channels?

CHECK
1. Timebase
2. X amplifier.
3. Check calibrator.

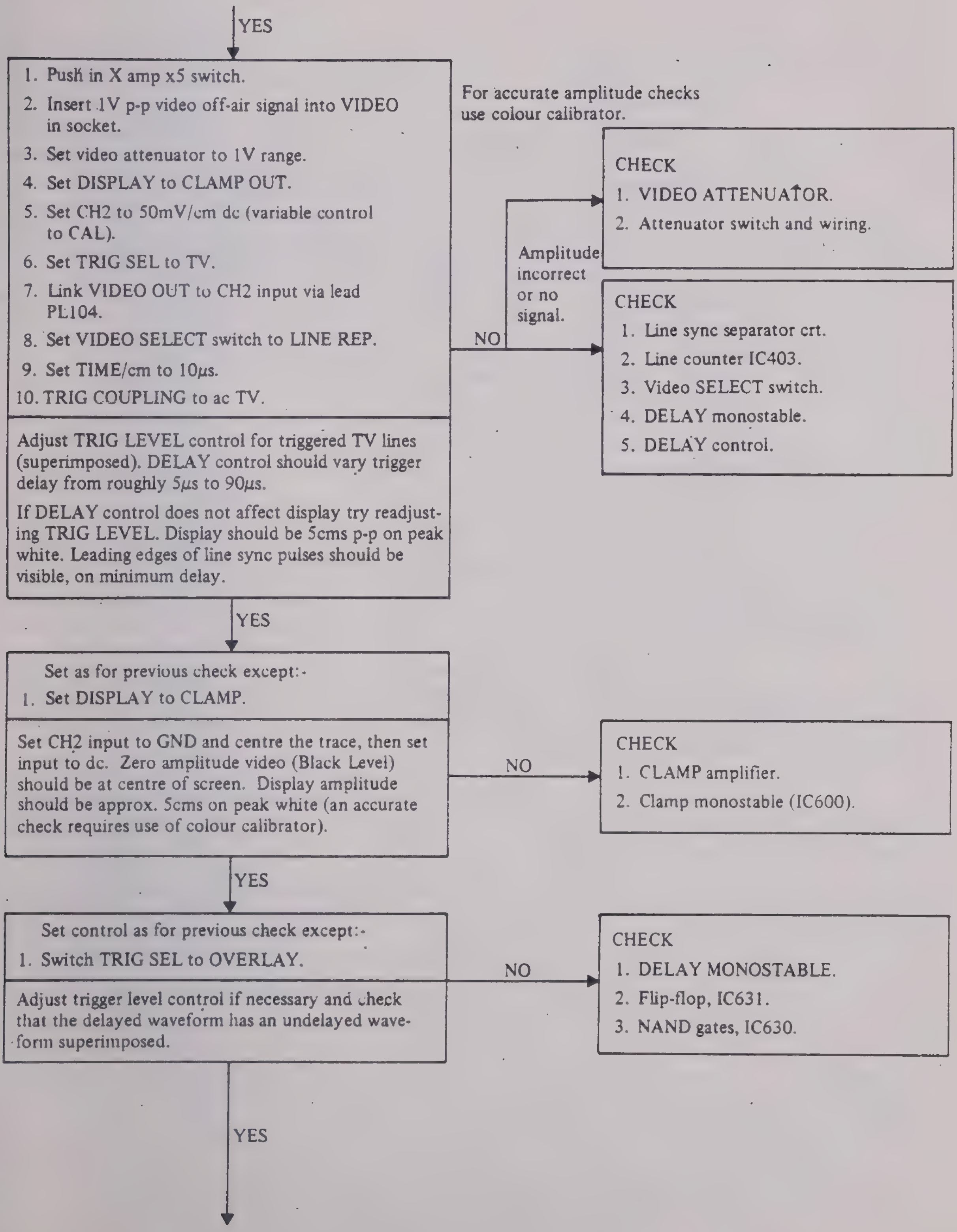
CHECK
1. Appropriate Y channel circuit.
2. Remaining Y amplifier circuits.
3. Check calibrator.

CHECK
1. Appropriate Y trigger amplifier.
2. Trigger course switch.
3. Timebase trigger amp.
4. Remaining Timebase circuit.

Set as for previous check except:-
1. TIME/cm to 5ms.
2. Set X amp. PULL x5.

Check for 1 cycle/two cms.

CHECK
1. Pull x5 switch and wiring.
2. X amplifier.



1. Push in X amp x5 switch.
2. Insert 1V p-p video off-air signal into VIDEO in socket.
3. Set video attenuator to 1V range.
4. Set DISPLAY to CLAMP OUT.
5. Set CH2 to 50mV/cm dc (variable control to CAL).
6. Set TRIG SEL to TV.
7. Link VIDEO OUT to CH2 input via lead PL104.
8. Set VIDEO SELECT switch to LINE REP.
9. Set TIME/cm to 10μs.
10. TRIG COUPLING to ac TV.

Adjust TRIG LEVEL control for triggered TV lines (superimposed). DELAY control should vary trigger delay from roughly 5μs to 90μs.

If DELAY control does not affect display try readjusting TRIG LEVEL. Display should be 5cms p-p on peak white. Leading edges of line sync pulses should be visible, on minimum delay.

For accurate amplitude checks use colour calibrator.

CHECK
1. VIDEO ATTENUATOR.
2. Attenuator switch and wiring.

CHECK
1. Line sync separator crt.
2. Line counter IC403.
3. Video SELECT switch.
4. DELAY monostable.
5. DELAY control.

Set as for previous check except:-
1. Set DISPLAY to CLAMP.

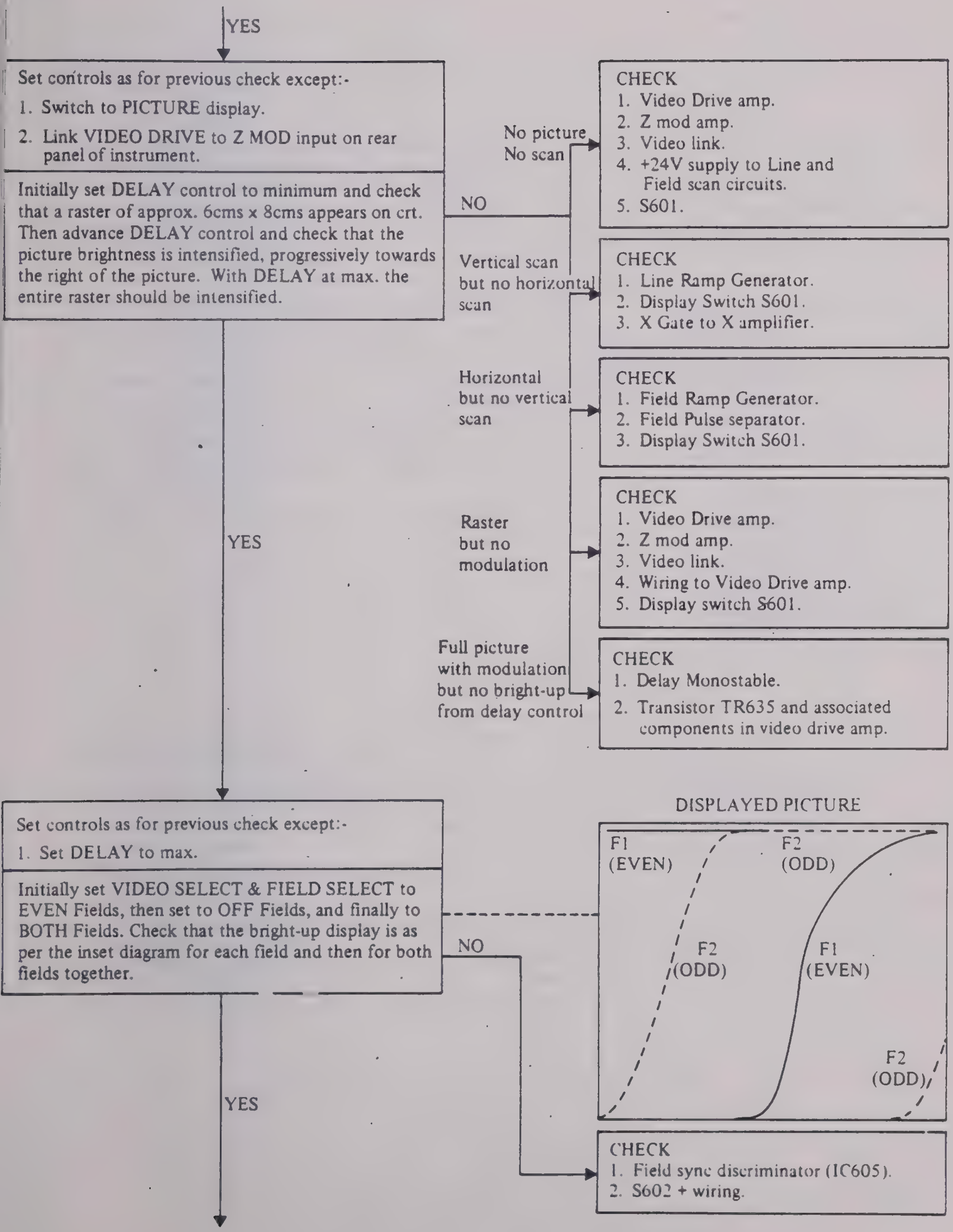
Set CH2 input to GND and centre the trace, then set input to dc. Zero amplitude video (Black Level) should be at centre of screen. Display amplitude should be approx. 5cms on peak white (an accurate check requires use of colour calibrator).

CHECK
1. CLAMP amplifier.
2. Clamp monostable (IC600).

Set control as for previous check except:-
1. Switch TRIG SEL to OVERLAY.

Adjust trigger level control if necessary and check that the delayed waveform has an undelayed waveform superimposed.

CHECK
1. DELAY MONOSTABLE.
2. Flip-flop, IC631.
3. NAND gates, IC630.



YES

Set controls as for previous check except:-

1. Switch to PICTURE display.
2. Link VIDEO DRIVE to Z MOD input on rear panel of instrument.

Initially set DELAY control to minimum and check that a raster of approx. 6cms x 8cms appears on crt. Then advance DELAY control and check that the picture brightness is intensified, progressively towards the right of the picture. With DELAY at max. the entire raster should be intensified.

NO

No picture
No scan

CHECK
1. Video Drive amp.
2. Z mod amp.
3. Video link.
4. +24V supply to Line and Field scan circuits.
5. S601.

Vertical scan but no horizontal scan

CHECK
1. Line Ramp Generator.
2. Display Switch S601.
3. X Gate to X amplifier.

Horizontal but no vertical scan

CHECK
1. Field Ramp Generator.
2. Field Pulse separator.
3. Display Switch S601.

Raster but no modulation

CHECK
1. Video Drive amp.
2. Z mod amp.
3. Video link.
4. Wiring to Video Drive amp.
5. Display switch S601.

Full picture with modulation but no bright-up from delay control

CHECK
1. Delay Monostable.
2. Transistor TR635 and associated components in video drive amp.

YES

Set controls as for previous check except:-

1. Set DELAY to max.

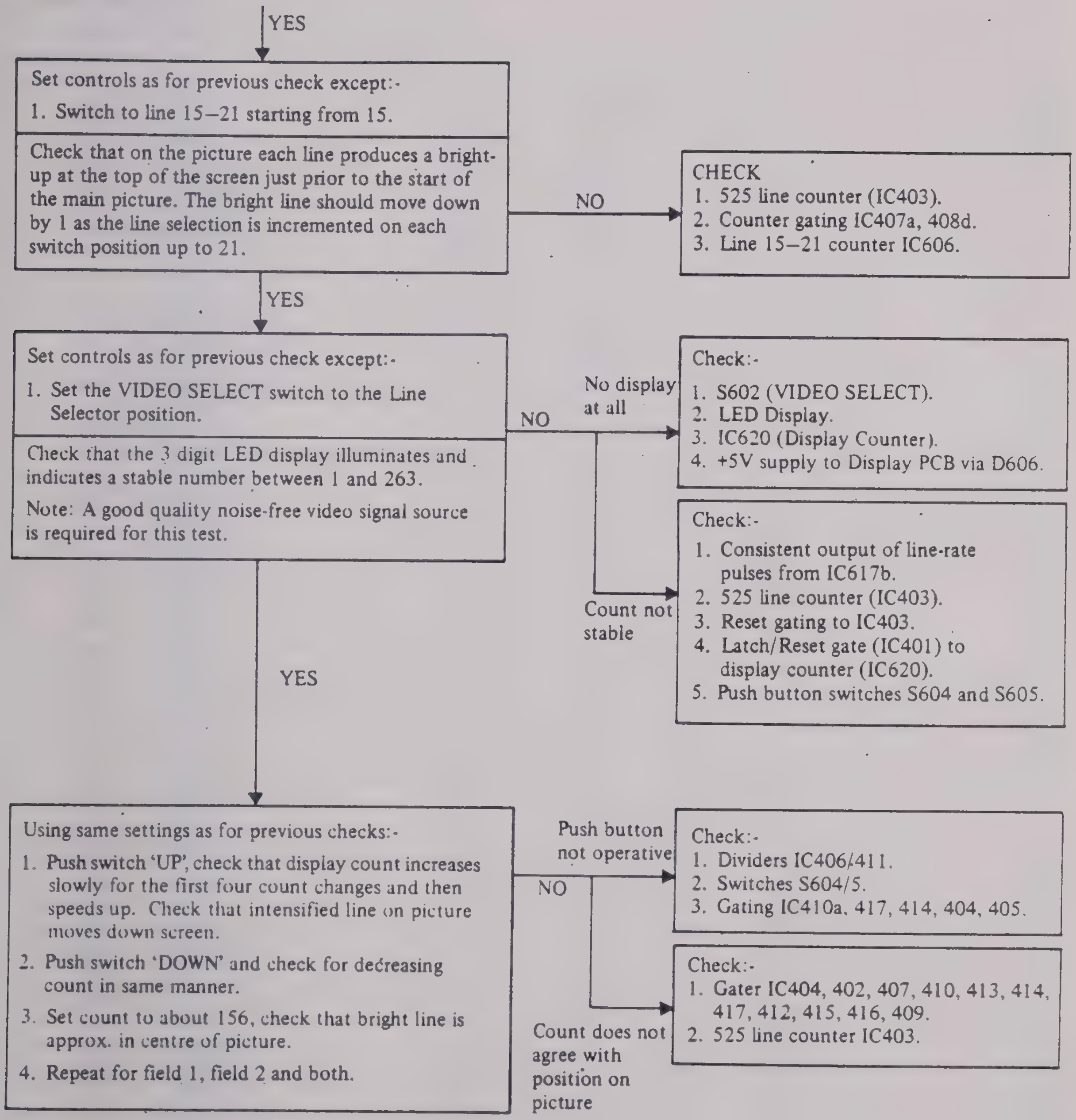
Initially set VIDEO SELECT & FIELD SELECT to EVEN Fields, then set to OFF Fields, and finally to BOTH Fields. Check that the bright-up display is as per the inset diagram for each field and then for both fields together.

NO

CHECK
1. Field sync discriminator (IC605).
2. S602 + wiring.

YES

DISPLAYED PICTURE


YES
NO
YES
NO
No display at all
Count not stable
YES
Push button not operative
NO
Count does not agree with position on picture

Set controls as for previous check except:-

1. Switch to line 15–21 starting from 15.

Check that on the picture each line produces a bright-up at the top of the screen just prior to the start of the main picture. The bright line should move down by 1 as the line selection is incremented on each switch position up to 21.

CHECK
1. 525 line counter (IC403).
2. Counter gating IC407a, 408d.
3. Line 15–21 counter IC606.

Set controls as for previous check except:-

1. Set the VIDEO SELECT switch to the Line Selector position.

Check that the 3 digit LED display illuminates and indicates a stable number between 1 and 263.

Note: A good quality noise-free video signal source is required for this test.

Check:-
1. S602 (VIDEO SELECT).
2. LED Display.
3. IC620 (Display Counter).
4. +5V supply to Display PCB via D606.

Check:-
1. Consistent output of line-rate pulses from IC617b.
2. 525 line counter (IC403).
3. Reset gating to IC403.
4. Latch/Reset gate (IC401) to display counter (IC620).
5. Push button switches S604 and S605.

Using same settings as for previous checks:-
1. Push switch 'UP', check that display count increases slowly for the first four count changes and then speeds up. Check that intensified line on picture moves down screen.
2. Push switch 'DOWN' and check for decreasing count in same manner.
3. Set count to about 156, check that bright line is approx. in centre of picture.
4. Repeat for field 1, field 2 and both.

Check:-
1. Dividers IC406/411.
2. Switches S604/5.
3. Gating IC410a, 417, 414, 404, 405.

Check:-
1. Gater IC404, 402, 407, 410, 413, 414, 417, 412, 415, 416, 409.
2. 525 line counter IC403.

OS3350/5 PRE-AMP 1 & 2 AND GAIN SWITCHING

Ref	*Value*	*Description*	*Tol % ±*	*Part No*
RESISTORS				
R10	470	CP	With S13	34779
R11	500	CP		A4/31250
R101	270	CF		28720
R102	270	CF		28720
R103	3k3	CF		21803
R104	3k3	CF		21803
R105	1k2	CF		21800
R106	1k2	CF		21800
R107	1k	CF		21799
R108	4k7	CF		21805
R109	4k7	CF		21805
R110	47	CF		28714
R111	47	CF		28714
R112	680	CF		28723
R113	3k3	CF		21803
R114	3k3	CF		21803
R115	100	CF		21794
R116	10	CF		21793
R117	10	CF		21793
R118	56	CF		28715
R119	10	CF		21793
R120	3k9	CF		21804
R121	680	CF		28723
R122	1k	CF		21799
R123	100	CP		33700
R124	1k	CF		21799
R125	110	MO		28783
R126	Not Used			
R127	330	MO		26741
R128	330	MO		26741
R129	560	CF		21798
R130	10	CF		21793
R131	47	CF		28714
R132	390	MO		26740
R133	1k5	CF		21801
R134	390	MO		26740
R135	180	CF		21795
R136	100	PCP		39230
R137	680	CF		28723
R138	220	PCP		39231
R139	100	MO		26747
R140	100	MO		26747
R141	10	CF		21793
R142	10	CF		21793
R143	100	CF		21794
R144	100	CF		21794
R145	2k2	CF		21802
R146	1k	PCP		39233
R147	2k2	CF		21802
R148	100	CF		21794
R149	100	CF		21794
R150	270	CF		28720
R151	270	CF		28720
R152				

Ref	*Value*	*Description*	*Tol % ±*	*Part No*
R153	10	CF		21793
R154	390	MO		26740
R155	390	MO		26740
R156	10	CF		21793
R157	10	CF		21793
R158	820	CF		28724
R159				
R160	27	CF		28711
R163	990k	MF		31927
R164				
R165	39	CF		28713
R166				
R167	10	CF		21793
R168	47	CF		28714
R169	10k1	MF		31928
R173	27	CF		28711
R174				
R175	10	CF		21793
R176	900k	MF	5	31929
R177	111k	MF	5	31930
R183	10	CF		21793
R184	10	CF		21793
R187	1M	MF	5	26346
R188				
R189	330k	CC		4408
R190	1k	CF		21799
R191	22Ω	CC	⅛W	28710
CAPACITORS				
C101	.01µF	CE(2)		22395
C102	.01µF	CE(2)		22395
C103	.01µF	CE(2)		22395
C104	.01µF	CE(2)		22395
C120	4.7pF	CE(2)		4502
C121		E		
C122	3/13pF	TRIMMER		32059
C123	.7/6pF	TRIMMER		29421
C124	220pF	CE(2)		22379
C125	220pF	CE(2)		22379
C126	.01µF	CE(2)		22395
C127	.01µF	CE(2)		22395
C128	.01µF	CE(2)		22395
C129	.01µF	CE(2)		22395
C130				
C131	.01µF	CE(2)		22395
C132	.01µF	CE(2)		22395
C133	.01µF	CE(2)		22395
C134	8.2pF	CE(2)		22363
C155	.1µF	CE(2)	400V	29495

DS3350/5 PRE-AMP 1 & 2 AND GAIN SWITCHING (Cont.)

Ref	Value	Description	Tol %±	Part No
CAPACITORS (Cont.)				
C156	47pF	CE(2)		22372
C157	10pF	CE(2)		4504
C158				
C159	.7/6pF	TRIMMER		25750
C160				
C161	.7/6pF	TRIMMER		25750
C162				
C163	330pF	CE(2)		31293
C164				
C165	.7/6pF	TRIMMER		25750
C166				
C167	.7/6pF	TRIMMER		25750
C168	47pF	CE(2)		29918
C171	.5/3pF	TRIMMER		42056
C172				
C173	5600pF	CE(2)		22394
TRANSISTORS				
TR101 TR102		AE12 Matched Pair		A31253
TR103 TR104		AE13 Matched Pair		A31254
TR120		2N2369		23307
TR121 TR122		AE13 Matched Pair		A31254

Ref	Value	Description	Tol %±	Part No
TR123		FTR129		40315
TR124		FTR129		40315
TR125		FTR129		40315
TR126		FTR129		40315
DIODES				
D101		FD300		35592
D102		FD300		35592
D103	6V2	ZENER		33930
D104	6V2	ZENER		33930
D120	7V5	ZENER		22173
D121	5V6	ZENER		33929
D122	5V1	ZENER		20218
D123	209A	L.E.D. T.I.L.		35202
MISCELLANEOUS				
L101				26986
S10				A2/31292
S11				35470
S12				
S13			With R10	34779
SKY				1222

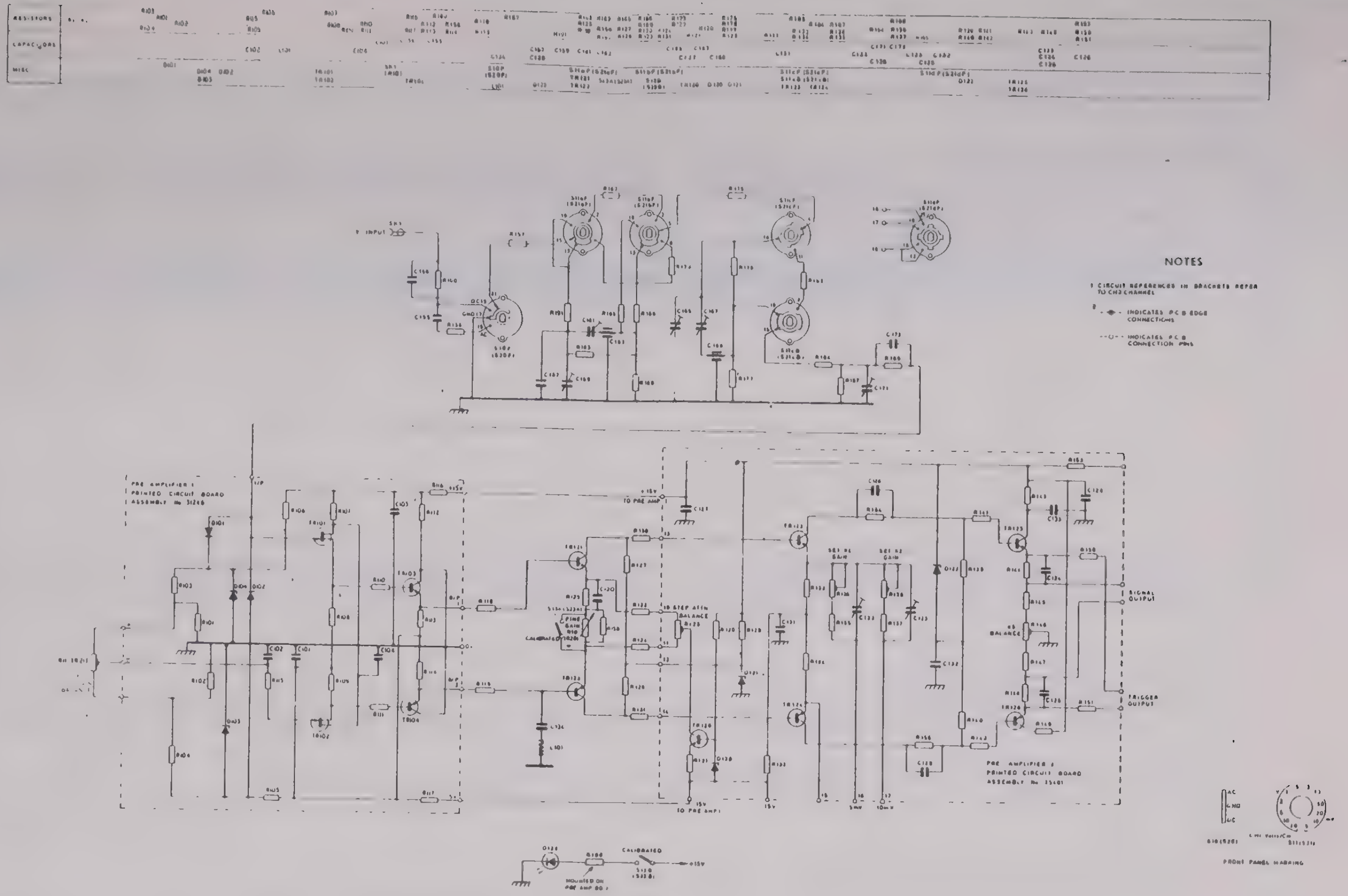

RESISTORS
CAPACITORS
MISC
INPUT
SK1
NOTES
1 CIRCUIT REFERENCES IN BRACKETS REFER TO CH2 CHANNEL
2 INDICATES P C B EDGE CONNECTIONS
INDICATES P C B CONNECTION PINS
PRE AMPLIFIER 1 PRINTED CIRCUIT BOARD ASSEMBLY No 31266
PRE AMPLIFIER 1 PRINTED CIRCUIT BOARD ASSEMBLY No 31601
+15V TO PRE AMP
15V TO PRE AMP
SET X1 GAIN
SET X2 GAIN
X2 STEP ATTN BALANCE
FINE GAIN
CALIBRATED
BALANCE
SIGNAL OUTPUT
TRIGGER OUTPUT
MOUNTED ON PRE AMP BD 1
+15V
AC
GND
DC
FRONT PANEL MARKING

Fig. 2 Circuit Diagram Pre-amp 1 & 2 and Gain Switching

OS3350/5 DELAY LINE DRIVER & BEAM SWITCH

Ref	*Value*	*Description*	*Tol %±*	*Part No*	*Ref*	*Value*	*Description*	*Tol %±*	*Part No*
RESISTORS									
R200	10	CF		21793	R255	1k8	CF		28725
R201	10	CF		21793	R256	22	CF		28710
R202	10	CF		21793	R257	1k2	MO		26734
R203	270	MO		26742	R258	10	CF		21793
R204	10	CF		21793	R259	10	CF		21793
R205	10	CF		21793	R260	47	CF		28714
R206	270	MO		26742	R261	120	CF		28718
R207	10	CF		21793	R262	390	MO		26740
R208	10	CF		21793	R263	39	CF		28713
R209	10	CF		21793	R264	39	CF		28713
R210	10	CF		21793	R265	180	CF A.O.T.		21795
R211	10	CF		21793	R266	56	CF		28715
R212	56	CF		28715	R267	150	CF		28719
R213	100	PCP		28520	R268	1k	CF		21799
R214	220	MO		26743	R269	4k7	CF		21805
R215	1k5	CF		21801	R270	820	CF		28724
R216	330	MO		26741	R271	3k9	CF		21804
R217	180	CF		21795	R272	3k9	CF		21804
R218	330	MO		26741	R273	820	CF		28724
R219	330	MO		26741	R274	10	CF		21793
R220					R275	10	CF		21793
R221	330	MO		26741	R276	4k7	CF		21805
R222	56	CF		28715	R277	1k	CF		21799
R223	100	PCP		28520	R278	150	CF		28719
R224	220	MO		26743	R279	390	CF		28722
R225	1k5	CF		21801	R280	10k	CF		21809
R226	680	CF		28723	R281	2k2	CF		21802
R227	2k2	PCP		24561	R282	3k3	CF		21803
R228	68	CF		28716	R283	3k9	CF		21804
R229	100	PCP		28520	R284	1k8	CF		28725
R230	220	CF A.O.T.		21796	R285	2k4	MO		26729
R231	2k2	PCP		24561	R286	470	CF		21797
R232	680	CF		28723	R287	2k7	CF		28726
R233	100	PCP		28520	R288	10	CF		21793
R234	68	CF		28716	R289	10	CF		21793
R235	100	CF A.O.T.		21794	R290	10	CF		21793
R236	68	CF		28716	R291	47	CF		28714
R237	470	CF		21797	R292	47	CF		28714
R238	470	PCP		28524	R293				
R239	39k	CF		28278	R294		A.O.T.		
R240	1k8	CF		28725	R295		A.O.T.		
R241					R296	100	CF		21794
R242	2k2	CF		21802					
R243	15k	CF		28727	**CAPACITORS**				
R244					C200	100pF	CE(2)		22376
R245	3k9	MO		26724	C201	.01μF	CE(2)		22395
R246	3k9	MO		26724	C202	3.5/13pF	TRIMMER		18803
R247	470	MO		26739	C203	.1μF	CE(1)	30V	19647
R248	470	MO		26739	C204	100pF	CE(2)		22376
R249	330	MO		26741	C205	.1μF	CE(1)	30V	19647
R250	330	MO		26741	C206	3.5/13pF	TRIMMER		18803
R252									
R252	820	MO		26736	C209	15pF	CE(2)		22366
R253	820	MO		26736	C210	15pF	CE(2)		22366
R254	22	CF		28710	C211	10/40pF	TRIMMER		29483

DS3350/5 DELAY LINE DRIVER & BEAM SWITCH (Cont.)

Ref	Value	Description	Tol %±	Part No
CAPACITORS (Cont.)				
C212	470pF	CE(2)		22383
C213	33pF	CE(2)		22370
C214	.01μF	CE(2)		22395
C215	22pF	CE(2)		22368
C216	22pF	CE(2)		22368
C217	.01μF	CE(2)		22395
C218	33pF	CE(2)		22370
C219	470pF	CE(2)		22383
C220	.01μF	CE(2)		22395
C221	900pF		1 125V	24885
C222	.01μF	CE(2)		22395
C223	47pF	CE(2)		22372
C224	.01μF	CE(2)		22395
C225	.1μF	CE(1)	30V	19647
C226	22μF	E	25V	32181
C227	3300pF	CE(2)		22391
C228	15pF	CE(2) A.O.T.		22366
C229	3300pF	CE(2)		22391
C230	150pF	CE(2)		22378
C231	150pF	CE(2)		22378
C232	100μF	E	25V	32183
TRANSISTORS				
TR201		AE16		A31781
TR202		AE16		A31781
TR203		AE16		A31781
TR204		AE16		A31781

Ref	Value	Description	Tol %±	Part No
TR205 TR206		AE17 Matched Pair		A32063
TR207		AE16		A31781
TR208		AE16		A31781
TR209		2N2369 I.T.T. Only		33701
TR210		2N2369 I.T.T. Only		33701
TR211		2N2369 I.T.T. Only		33701
TR212		AE16		A31781
TR213		AE16		A31781
TR214		AE16		A31781
TR215		2N2369 I.T.T. Only		33701
TR216		2N2369 I.T.T. Only		33701
TR217		2N2369 I.T.T. Only		33701
TR218		2N2369 I.T.T. Only		33701
DIODES				
D201		1N916		1949
D202		1N916		1949
D203		1N916		1949
D204		1N916		1949
D205		1N916		1949
D206		1N916		1949
D207		1N916		1949
D208		1N916		1949
D209	5V6	ZENER		33929
D210				
D211		1N4148		23802
D212		1N4148		23802

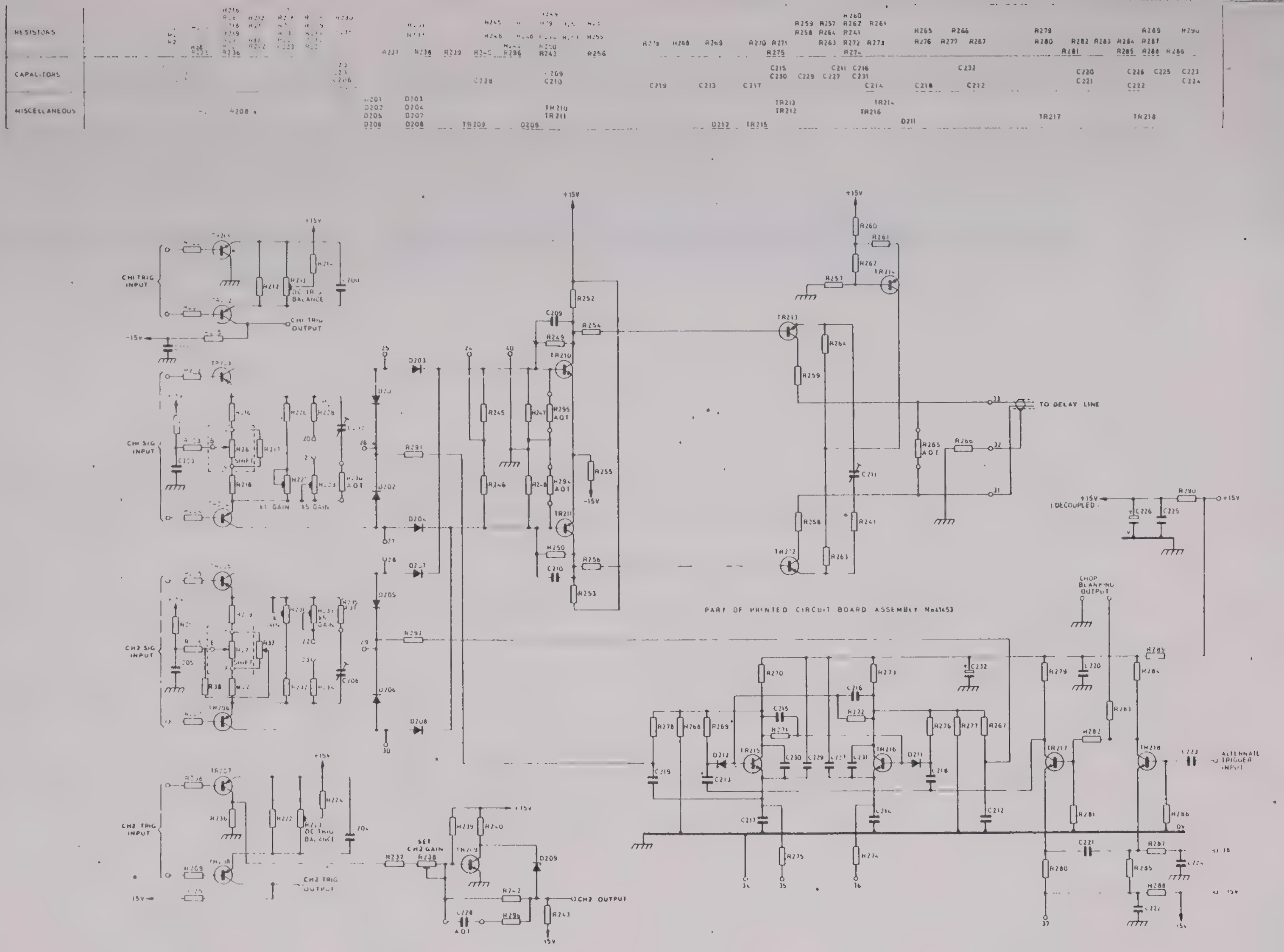

RESISTORS
CAPACITORS
MISCELLANEOUS
CH1 TRIG INPUT
CH1 TRIG OUTPUT
CH1 SIG INPUT
CH2 SIG INPUT
CH2 TRIG INPUT
CH2 TRIG OUTPUT
DC TRIG BALANCE
X1 GAIN
X5 GAIN
SHIFT
SET CH2 GAIN
CH2 OUTPUT
+15V
-15V
TO DELAY LINE
+15V (DECOUPLED)
PART OF PRINTED CIRCUIT BOARD ASSEMBLY No41453
CHOP BLANKING OUTPUT
ALTERNATE TRIGGER INPUT
0V
AOT

Fig. 3 Circuit Diagram Delay Line Driver and Beam Switch

OS3350/5 DELAY EQUALISER & OUTPUT DRIVER

RESISTORS

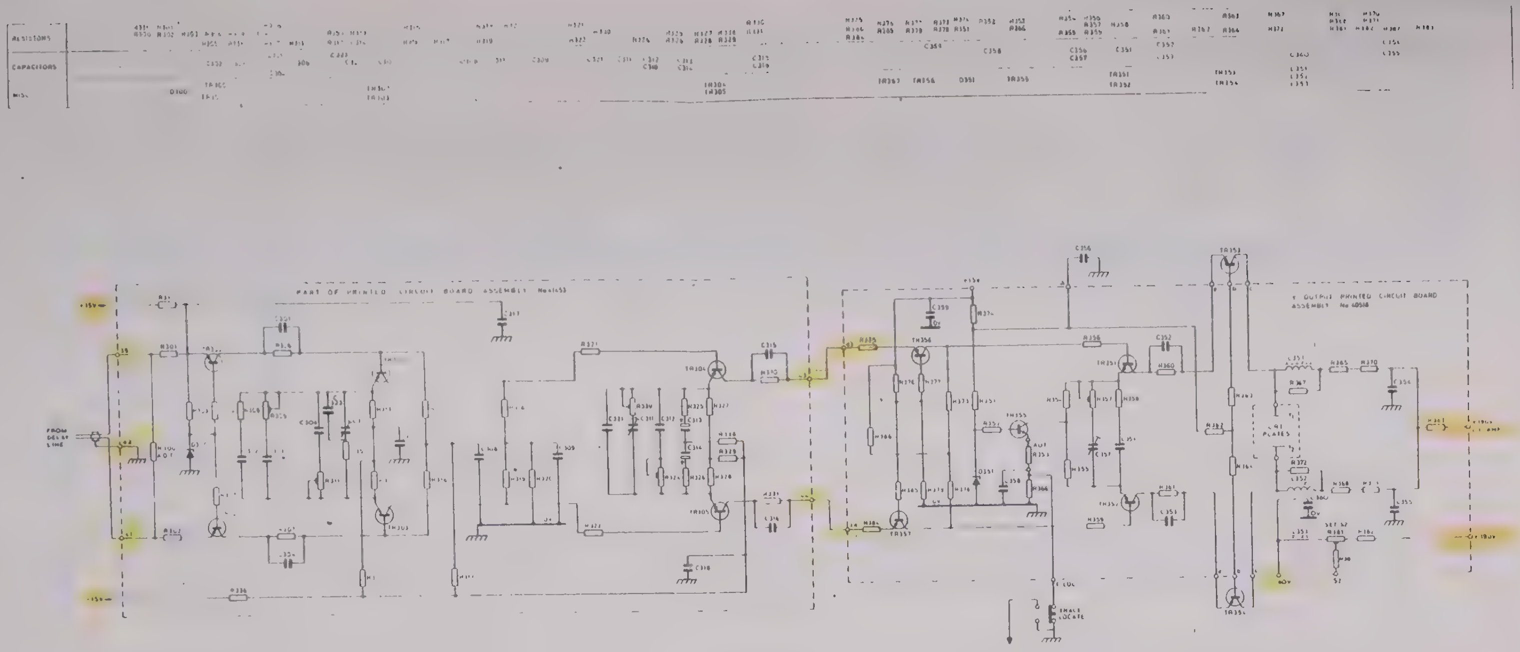
Ref	*Value*	*Description*	*Tol %±*	*Part No*
R300	1k8	CF	A.O.T.	28725
R301	100	MO		26747
R302	100	MO		26747
R303	3k3	CF		21803
R304	22	CF		28710
R305	22	CF		28710
R306	390	MO		26740
R307	390	MO		26740
R308	12k	CF		21810
R309	22k	PCP		25885
R310				
R311	10k	PCP		28525
R312	390	MO		26740
R313	39	CF		28713
R314	39	CF		28713
R315	100	CF		21794
R316	100	CF		21794
R317	560	MO		36737
R318	100	MO		26747
R319	100	MO		26747
R320	47	CF		28714
R321	22	CF		28710
R322	22	CF		28710
R323				
R324	2k2	PCP		24561
R325	3k3	CF		21803
R326	3k3	CF		21803
R327	56	MO		28777
R328	56	MO		28777
R329	560	MO		26737
R330	150	MO		26745
R331	150	MO		26745
R335	10	CF		21793
R336	10	CF		21793
R337				
R338	100k	CF		21819
R339	220	PCP		36262
R350	10	CF		21793
R351	2k2	CF		21802
R352	47	CF		28714
R353	51	MF	2W	38563
R354	56	MO		28777
R355	56	MO		28777
R356	10	CF		21793
R357	100	PCP		28520
R358	270	CF		28720
R359	10	CF		21793
R360	56	MO		28777
R361	56	MO		28777
R362	56	CF		28715
R363	56	CF		28715
R364	56	CF		28715
R365	680	MO	5 2W	40452
R366	270	CF		28720
R367	3k3	CF		21803
R368	680	MO	5 2W	40452
R369				
R370	680	MO	5 2W	40452
R371	680	MO	5 2W	40452
R372	3k3	CF		21803
R373	270	CF		28720
R374	10	CF		21793
R375	100	CF		21794
R376	1k8	CF		28725
R377	10	CF		21793
R378	270	CF		28720
R379	680	CF		28723
R380				
R381	220k	PCP		29363
R382	120k	CF		21820
R383	1k5	WW		598
R384	100	CF		21794
R385	10	CF		21793
R386	150	CF		28719
R387	2.2k	MO		26730

CAPACITORS

Ref	*Value*	*Description*	*Tol %±*	*Part No*
C301	1000pF	CE(2)		22387
C302	.22μF	PE	160V	31379
C303	82pF	CE(2)		22375
C304	1000pF	CE(2)		22387
C305				
C306	47pF	CE(2)		22372
C307	.01μF	CE(2)	250V	22395
C308	.01μF	CE(2)	250V	22395
C309	.01μF	CE(2)	250V	22395
C310				
C311	10/40pF	TRIMMER		29483
C312	27pF	CE(2)		22369
C313	33μF	E	16V	32173
C314	33μF	E	16V	32173
C315	1000pF	CE(2)		22387
C316	1000pF	CE(2)		22387
C317	.01μF	CE(2)	250V	22395
C318	.01μF	CE(2)	250V	22395
C321	4.7pF	CE(2)		4502
C322	3.5/13pF	TRIMMER		18803
C351	27pF	CE(2)		22369
C352	100pF	CE(2)		22376
C353	100pF	CE(2)		22376
C354	.01μF	CE(2)	250V	22395
C355	.01μF	CE(2)	250V	22395
C356	.01μF	CE(2)	250V	22395
C357	10/60pF	TRIMMER		37347
C358	.01μF	CE(2)	250V	22395
C359	.01μF	CE(2)	250V	22395
C360	.01μF	CE(2)	250V	22395

S3350/5 DELAY EQUALISER & OUTPUT DRIVER (Cont.)

Ref	Value	Description	Tol %±	Part No
TRANSISTORS				
TR300		AE16		A31781
TR301		AE16		A31781
TR302		2N2369	I.T.T. Only	33701
TR303		2N2369	I.T.T. Only	33701
TR304		2N2369	I.T.T. Only	33701
TR305		2N2369	I.T.T. Only	33701
TR351		2TX327	I.T.T. Only	39271
TR352		2N2369	I.T.T. Only	33701
TR353		BD529		35840
TR354		BD529		35840
TR355		2N2369	I.T.T. Only	33701
TR356		2N2369	I.T.T. Only	33701
TR357		2N2369	I.T.T. Only	33701
DIODES				
D300	3V9	ZENER		33925
D351	3V3	ZENER		33923
MISCELLANEOUS				
L351	6.8µH			40451
L352	6.8µH			40451
L353		Ferrite FX1242		26986


RESISTORS
CAPACITORS
MISC.
FROM DELAY LINE
+15V
-15V
PART OF PRINTED CIRCUIT BOARD ASSEMBLY
Y OUTPUT PRINTED CIRCUIT BOARD ASSEMBLY
TR304
TR305
TR351
TR352
TR353
TR354
TR355
TR356
TR357
R335
R336
R371
R372
R365
R370
R367
R368
R360
C315
C316
C352
C354
C355
C356
C359
L351
L352
D351
CRT PLATES
TRACE LOCATE

NOTES

– – – INDICATES PCB CONNECTION PINS

Fig. 4 Circuit Diagram Delay Equaliser and Output Driver

OS3350/5 TIMEBASE P.C.

Ref	*Value*	*Description*	*Tol % ±*	*Part No*	*Ref*	*Value*	*Description*	*Tol % ±*	*Part No*
RESISTORS									
R400	47	CF	¼W	28714	R455	3k3	CF	¼W	21803
R401	100k	CF	1W	19061	R456	1k5	CF	¼W	21801
R402	2k2	CF	¼W	21802	R457	100	CF	¼W	21794
R403	10	CF	¼W	21793	R458	5k6	CF	¼W	21806
R404	47	CF	¼W	28714	R459	10	CF	¼W	21793
R405	47	CF	¼W	28714	R460	10	CF	¼W	21793
R406	47	CF	¼W	28714	R461	330	CF	¼W	28721
R407	4k7	CF	¼W	21805	R462	33k	CF	¼W	21814
R408	1k5	CF	¼W	21801	R463	10	CF	¼W	21793
R409	10k	CF	¼W	21809	R464	10	CF	¼W	21793
R410	1k	CF	¼W	21799	R465	820	CF	¼W	28724
R411	3k9	CF	¼W	21804	R466	22k	CF	¼W	21812
R412	100	CF	¼W	21794	R467	470	CF	¼W	21797
R413	2k7	CF	¼W	28726	R468	220k	CF	¼W	21823
R414	220	CF	¼W	21796	R469	470	CF	¼W	21797
R415	1k5	CF	¼W	18552	R470	390	CF	¼W	28722
R416	560	CF	¼W	21798	R471	4k7	CF	¼W	21805
R417	8k2	CF	¼W	21808	R472	2k7	CF	¼W	28726
R418	470k	CF	¼W	32330	R473	10	CF	¼W	21793
					R474	220	CF	¼W	21796
R420	10k	CF	¼W	21809	R475	1k	CF	¼W	21799
R421	220k	CF	¼W	21823	R476	1k5	CF	½W	18552
R422	33k	CF	¼W	21814	R477	91	MO		28782
R423	22k	CF	¼W	21812	R478	1k2	CF	¼W	21800
R424	1k8	CF	¼W	28725	R479	8k2	CF	¼W	21808
R425	33k	CF	¼W	21814					
R426	1k	CF	¼W	21799	R481	180k	CF	¼W	21822
R427	1k	CF	¼W	21799	R482	1k2	CF	¼W	21800
R428	100k	CF	¼W	21819	R483	22k	CF	¼W	21812
R429	470	CF	¼W	21797	R484	4k7	CF	¼W	21805
R430	560k	CF	¼W	32359	R485	620	MO		22485
R431	100	CF	¼W	21794	R486	22k	CF	¼W	21812
R432	4k7	CF	¼W	21805	R487	1k8	CF	¼W	28725
R433	150k	CF	¼W	21821	R488	10	CF	¼W	21793
R434	3k9	CF	¼W	21804	R489	750	MO		28790
R435	39	CF	¼W	28713	R490	10	CF	¼W	21793
R436	47	CF	¼W	28714	R491	470	CF	¼W	21797
R437	12k	CF	¼W	21820	R492	4k7	CF	¼W	21805
R438	100	CF	¼W	21794	R493	820	CF	¼W	28724
R439	10	CF	¼W	21793	R494	100k	CF	¼W	21819
R440	100k	CP Part of switch, trigger			R495	1k5	CF	¼W	21801
		With S40/41		42607	R496	10	CF	¼W	21793
R441	4k7	CF	¼W	21805	R497	10	CF	¼W	21793
R442	22	CF	¼W	28710	R498	120k	CF	¼W	21820
R443	3k3	CF	¼W	21803	R499	8k2	CF	¼W	21808
R444	4k7	CF	¼W	21805	R500	6k8	CF	¼W	21807
R445	1k5	CF	¼W	21801	R501	820	CF	¼W	28724
					R502	100k	CF	¼W	21819
R447	100k	CF	¼W	21819					
R448	27k	CF	¼W	21813	R504	3k3	CF	¼W	21803
					R505	1k2	CF	¼W	21800
R450	4k7	CF	¼W	21805	R506	4k7	CF	¼W	21805
R451	47	CF	¼W	28714	R507	10k			A4/34780
R452	680	CF	¼W	28723	R508	4k7	CF	¼W	21805
R453	1k	PCP	5 ¼W	26870	R509	1k2	CF	¼W	21800
R454	1k3	MO		28792	R510	470	PCP		28524

S3500/5 TIMEBASE P.C. (Cont.)

ESISTORS (Cont.)

ef	Value	Description	Tol %±	Part No
511	10k	CF	¼W	21809
512	3k3	MO		26726
513	100	CF	¼W	21794
514	3k3	MO		26726
R515	100	CF	¼W	21794
R516	10k	CF	¼W	21809
R517	10k	CF	¼W	21809
R518	8k2	CF	¼W	21808
R519	10k	CF	¼W	21809
R520	10k	CF	¼W	21809
R521	10k	CF	¼W	21809
R522	10k	CF	¼W	21809
R523	100	CF	¼W	21794
R524	47k	CF	¼W	21815
R525	6k8	CF	¼W	21807
R526	470	CF	¼W	21797
R527	100	CF	¼W	21794
R529	1k5	CF	¼W	21801
R530	10k	CF	¼W	21809
R532	390	CF	½W	18545
R533	6k8	CF	¼W	21807
R534	1k	CF	¼W	21799
R535	4k7	CF	¼W	21805
R536	1k	CF	¼W	21799
R537	10	CF	¼W	21793
R538	10M	CC		1179
R539	47	CF	¼W	28714
R540	4k7	CF	¼W	21805
R541	10k	CF	¼W	21809
R542	6k8	CF	¼W	21807
R543	4k7	CF	¼W	21805
R544	1k3	CF	¼W	33338
R545	100	CF	¼W	21794
R546	47	CF	¼W	28714
R547	47	CF	¼W	28714
R548	100k	CF	¼W	21819
R549	2k7	CF	¼W	28726
R550	10	CF	¼W	21793
R551	390	CF	¼W	28722
R552	100k	CF	¼W	21819
R553	2k	MO		26731
R554	680	CF	¼W	28723
R555	1k	CF	¼W	21799
R556	1k8	CF	¼W	28725
R557	33	CF	¼W	28712
R558	47	CF	¼W	28714
R559	100	CF	¼W	21794
R560	47k	CF	¼W	21815
R561				
R562				
R563		Shown on Interconnect Circuit Drawing SK2765		
R564				
R565				
R566				

Ref	Value	Description	Tol %±	Part No
R567				
R568		Shown on Interconnect Circuit Drawing SK2765		
R569				
R570				
R571	22	CF	¼W	28710
R573	15	CF	¼W	28708
R574	3k9	CF	¼W	21804
R575		See SK2765		
R576	100	CF	¼W	21794
R577	470	CF	¼W	21797
		A.O.T.		
R579	15	CF	¼W	28708
R590	10k	CF	¼W	21809
R591	10k	CF	¼W	21809
R592	10k	CF	¼W	21809
R593	10k	CF	¼W	21809
R594	10k	CF	¼W	21809
R595	10k	CF	¼W	21809
R596	10k	CF	¼W	21809
R597	10k	CF	¼W	21809

CAPACITORS

Ref	Value	Description	Tol %±	Part No
C400	47pF	SM		4502
C401	220pF	CE(2)		22379
C402	.47μF	PE	160V	31381
C403	470pF	CE(2)		22383
C404	33pF	CE(2)		22370
C405	100pF	CE(2)		22376
C406	10pF	CE(2)		22364
C407	33pF	CE(2)		22370
C408	47pF	CE(2)		22372
C409	.01μF	CE(2)		22395
C410	1000pF	CE(2)		22387
C411	.1μF	CE(1)	250V	31377
C412	.1μF	CE(1)	250V	31377
C413	100pF	CE(2)		22376
C414	1000pF	CE(2)		22387
C415	220pF	CE(2)		22379
C417	.1μF	CE(2)	25V	36709
C418	.1μF	CE(2)	250V	31377
C419	.01μF	CE(2)		22395
C420	22pF	CE(2)		22368
C421	.1μF	CE(1)	25V	36709
C422	.1μF	CE(1)	25V	36709
C423	1000pF	CE(2)		22387
C424	390pF	CE(2)		22382
C425	22μF	E	25V	32181
C426	27pF	CE(2)		22369
C427	.01μF	CE(2)	250V	22395
C428	.01μF	CE(2)	250V	22395
C429	1.5pF	S/M		813
C430	22pF	CE(2)		22368
C431	18pF	CE(2)		22367

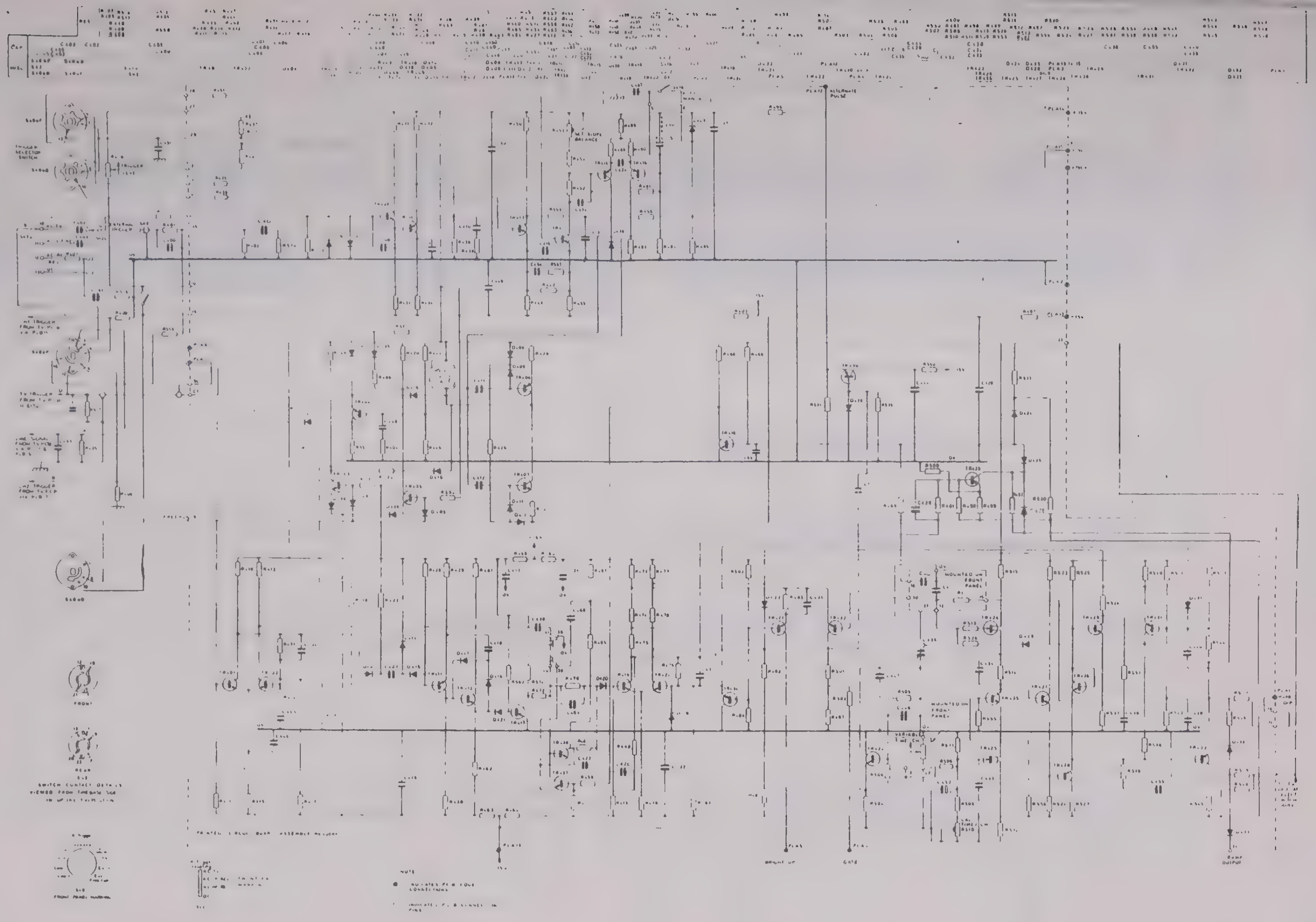

TRIGGER SELECTOR SWITCH
SLOPE BALANCE
ALTERNATE PULSE
MOUNTED ON FRONT PANEL
FRONT
REAR
SWITCH CONTACT DETAILS
BRIGHT UP
GATE
RAMP OUTPUT
NOTE

Fig. 5A Circuit Diagram Timebase

OS3350/5 TIMEBASE P.C. (Cont.)

CAPACITORS (Cont.)

Ref	Value	Description	Tol %±	Part No
C432	6.8pF	CE(2)		22362
C433	.01μF	CE(2)	250V	22395
C434	.01μF	CE(2)	250V	22395
C435	6/25pF	TRIMMER		23593
C438	100pF	CE(2)		22376
C439	.01μF	CE(2)	250V	22395
C440	33pF	CE(2)		22370
C444	.01μF	CE(2)	250V	22395
C445	150pF	CE(2)		22378
C446	.1μF	CE(1)	25V	36709
C447	220pF	CE(2)		22379
C448	.01μF	CE(2)	250V	22395
C449	.01μF	CE(2)	250V	22395
C450	.01μF	CE(2)	250V	22395
C451	.01μF	CE(2)	250V	22395
C452	33μF	E	16V	32175
C453	.01μF	CE(2)	250V	22395
C454	1000pF	CE(2)		22387
C455	22pF	CE(2)		22368
C456 C457 C458 C459 C460 C461		Shown on Interconnect Circuit Drawing SK2765		
C462	.01μF	CE(2)	250V	22395
C463	4.7pF	CE(2)		29649
C465	27pF	CE(2)		22369
C466	1500pF	CE(2)		22388
C467	.01μF	CE(2)	250V	22395
C480	470pF		10	42428
C481	470pF		10	42428
C483	470pF	CE(2)		42428
C484	.01μF	CE(2)	20	42444
C485	.01μF	CE(2)	20	42444
C486	.01μF	CE(2)	20	42444
C487	.01μF	CE(2)	20	42444
C488	.01μF	CE(2)	20	42444
C489	33μF	E	16V	32173
C490	100pF	CE(2)		42420
C491	100pF	CE(2)		42420

TRANSISTORS

Ref	Value	Description	Tol %±	Part No
TR401		BSX20		23307
TR402		BSX20		23307
TR403		BC107		26790
TR404		2N3906		21533
TR405		BC107		26790
TR406		2N3906		21533
TR407		BC108		26110
TR409		2N930		21548
TR410		2N3906		21533
TR411		2N3906		21533
TR412		BC107		26790
TR413 TR414		AE13 Matched Pair		A31254
TR415		MPS3640		24128
TR416		MPS3640		24128
TR417		BSX20		23307
TR418		BC108		26110
TR419		BSX20		23307
TR420		BSX20		23307
TR421		2N3906		21533
TR422		2N3906		21533
TR423		2N930		21548
TR424		BC108		26110
TR425 TR426		AE31 Matched Pair		A36243
TR427		BC107		26790
TR428		2N3906		21533
TR429 TR430		AE13 Matched Pair	With TR436	A31254
TR431		MPS3640		24128
TR432		2N3906		21533
TR434		MPS3640		24128
TR435		BSX20		23307
TR436		See TR429		
TR437		BSX20		23307
TR438		BSX20		23307

INTEGRATED CIRCUITS

Ref	Value	Description	Tol %±	Part No
IC401		4001		36195
IC402		4023		37812
IC403		4040		40506
IC404		4011		34953
IC405		4011		34953
IC406		4017		37689
IC407		4011		34953
IC408		4044		44024
IC409		4001		36195
IC410		4081		37694
IC411		4017		37689
IC412		4011		34953
IC413		4049		36200
IC414		4011		34953
IC415		4011		34953
IC416		4011		34953
IC417		4011		34953

DIODES

Ref	Value	Description	Tol %±	Part No
D401		IN4148	Selected	34701
D402		IN4148		23802
D403		IN4148		23802
D404		IN4148		23802
D405		IN4148		23802

S3350/5 TIMEBASE P.C. (Cont.)

ef	Value	Description	Tol %±	Part No
IODES (Cont.)				
D406		IN4148		23802
D407		IN4148		23802
D408		IN4148		23802
D409		IN4148		23802
D410		IN4148		23802
D411		IN4148		23802
D412		IN4148		23802
D414		OA47		4468
D415		OA47		4468
D416		IN4148		23802
D417		IN4148		23802
D418		IN4148		23802
D419		AAZ13		4472
D420		IN4148	Selected	34701
D421		IN4148		23802
D422		IN4148	Selected	34701
D423	6V8	ZENER		4666
D424		IN4148		23802
D425		OA47		4468
D426		IN4148		23802
D427		IN4148		23802
D428		IN4148		23802

Ref	Value	Description	Tol %±	Part No
D429		IN3595	Selected	34701
D431		IN4148	Selected	34701
D432		IN4148		23802
D433		IN4148		23802
D435		IN4148		23802
D436		IN4148		23802
D438		IN4148		23802
D439		IN4148		23802
D441		LED	See SK2765	
MISCELLANEOUS				
L402		Bead Ferrite FX1242		26986
S40			With R440	42607
S41				
S42				A3/35756
SKE		50Ω BNC		1222

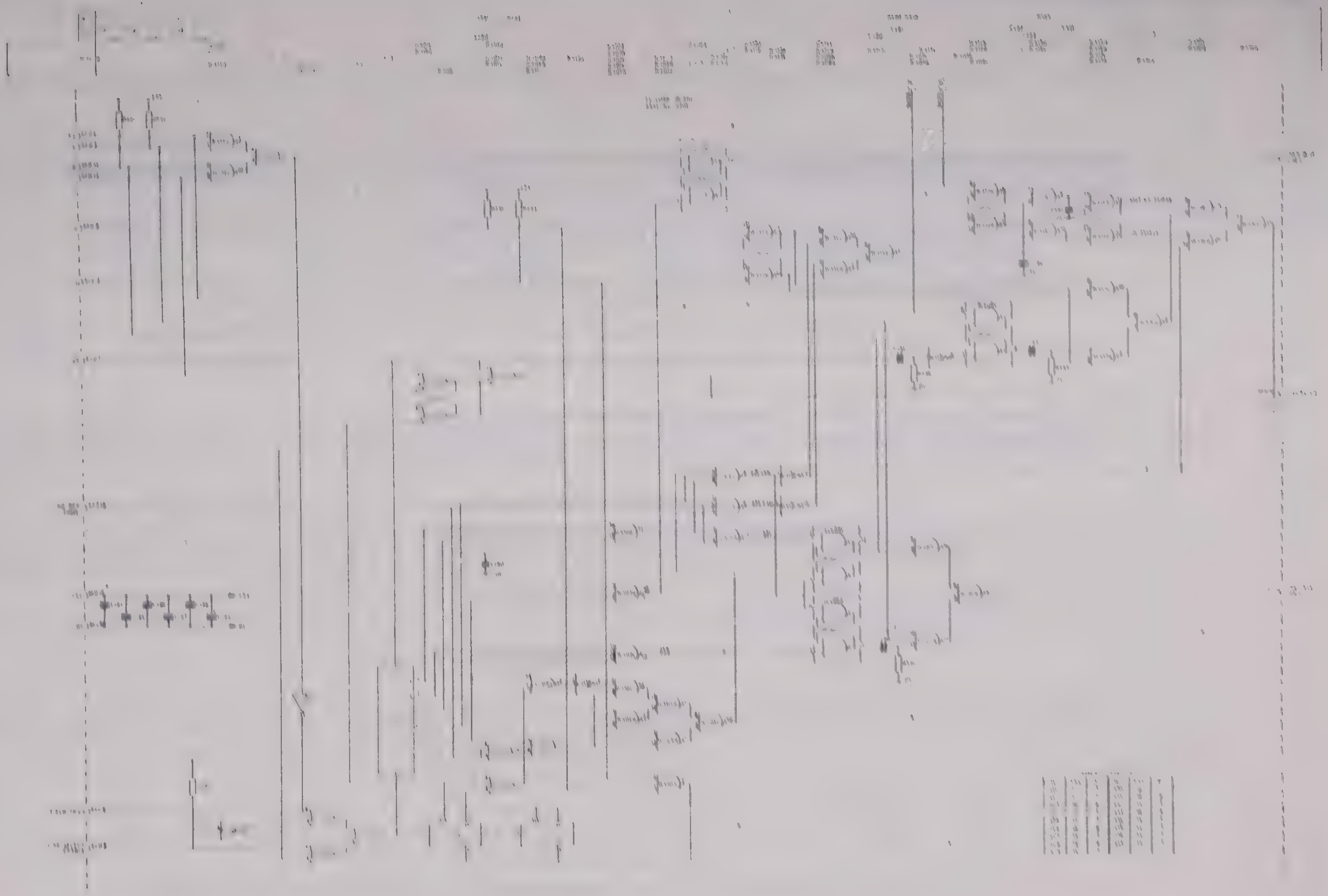


Fig 3d Circuit Diagram I V Unit

33350/5 T.V. SYNC

ef	Value	Description		Tol %±		Part No
ESISTORS						
600	24R9	MF		½		40523
601	24R9	MF		½		40523
602	100	MF		½		40524
603	75	MF		½		40525
604	75	MF		½		40525
605	44R9	MF		½		40527
606	44R9	MF		½		40527
607	40R2	MF		½		40522
608	150	MF		½		40526
R609	10	CF			¼W	21793
R610	43k	MF		2		38633
R611	7k5	MF		2		38615
R612	220	CF			¼W	21796
R613	1k5	CF			¼W	21801
R614						
R615	3k3	CF			¼W	21803
R616	680	CF			¼W	28723
R617	100	CP				40496
R618	390	MF		2		38584
R619	10M	CF		10	¼W	32661
R620	430	MF		2		38585
R621						
R622	68	CF			¼W	28716
R623						
R624	1k3	MF				38597
R625	2k7	CF	A.O.T.		¼W	28726
R626	820	MF		2		38592
R627	1k	MF		2		38594
R628	18k	MF	A.O.T.	2		38624
R629	5k1	MF		2		38611
R630	68	CF			¼W	28716
R631						
R632	220	MF		2		38578
R633	750	MF		2		38591
R634						
R635	75	MF		2		40710
R636	10k	CF			¼W	21809
R637	100k	CF			¼W	21819
R638	3k9	MF		2		38603
R639	2k	MF		2		38601
R640	11k	MF		2		38619
R641	10k	CF			¼W	21809
R642	10k	CF			¼W	21809
R643	10k	CF			¼W	21809
R644	1k8	MF		2		38600
R645	100	CF			¼W	21794
R646	120	WW			2.5W	40502
R647	560	CF			¼W	21798
R648	3k	MF		2		38605
R649	4k7	MF				38610
R650	820	MF		2		38592
R651	3k	MF		2		38605
R652	1k	CF			¼W	21799
R653	2k7	CF			¼W	28726
R654						
R655	100	CF			¼W	21794

Ref	Value	Description		Tol %±		Part No
R656	5k6	CF			¼W	21806
R657	330k	MF		2		38654
R658	5k1	MF		2		38611
R659	2k7	MF		2		38604
R660	1M	MF		2		40493
R661	1M8	MG		5		35752
R662	330	CF			¼W	28721
R663	56k	CF			¼W	28729
R664	5k6	CF			¼W	21806
R665	56k	MF		2		38636
R666	3k3	CF		5	¼W	21803
R667	4k7	CF			¼W	21805
R668	18k	MF		2		38624
R669	100	CF			¼W	21794
R670	5k6	CF			¼W	21806
R671	6k8	CF			¼W	21807
R672	100k	CF			¼W	21819
R673	10k	CF			¼W	21809
R674	75	MF		2		38567
R675	1k	MF		2		38594
R676	820	MF		2		38592
R677	1k2	MF		2		38596
R678	1k	CF			¼W	21799
R679	560	CF			¼W	21798
R680	1k	CF			¼W	21799
R681	2k2	CF			¼W	21802
R682	2k2	CF			¼W	21802
R683	4k7	CF			¼W	21805
R684	10	CF			¼W	21793
R685						
R686	3k3	CF			¼W	21803
R687	1k5	CF			¼W	21801
R688	2k2	CF			¼W	21802
R689	2k2	CF			¼W	21802
R690	220	CF			¼W	21796
R691	240	CF		2	¼W	38579
R692	10k	CF			¼W	21809
R693	39k	CF			¼W	28728
R694	1k	CF			¼W	21799
R695	3k3	CF			¼W	21803
R696	330	CF			¼W	28721
R697	10k	CF			¼W	21809
R698	1k	CP	With S76			35294
R699	1k	CP				
R700	30k	MF		2		38629
R701	20k	MF		2		38625
R706	6k8	MF		2		38614
R707	220	MF		2		38743
R708	430	MF		2		38585
R712	10k	CF			¼W	21809
R713	1k6	MF		2		38599
R714	25k	CP				[illegible]
R715	2k2	CF			¼W	21802
R716	2k2	CF			¼W	21802

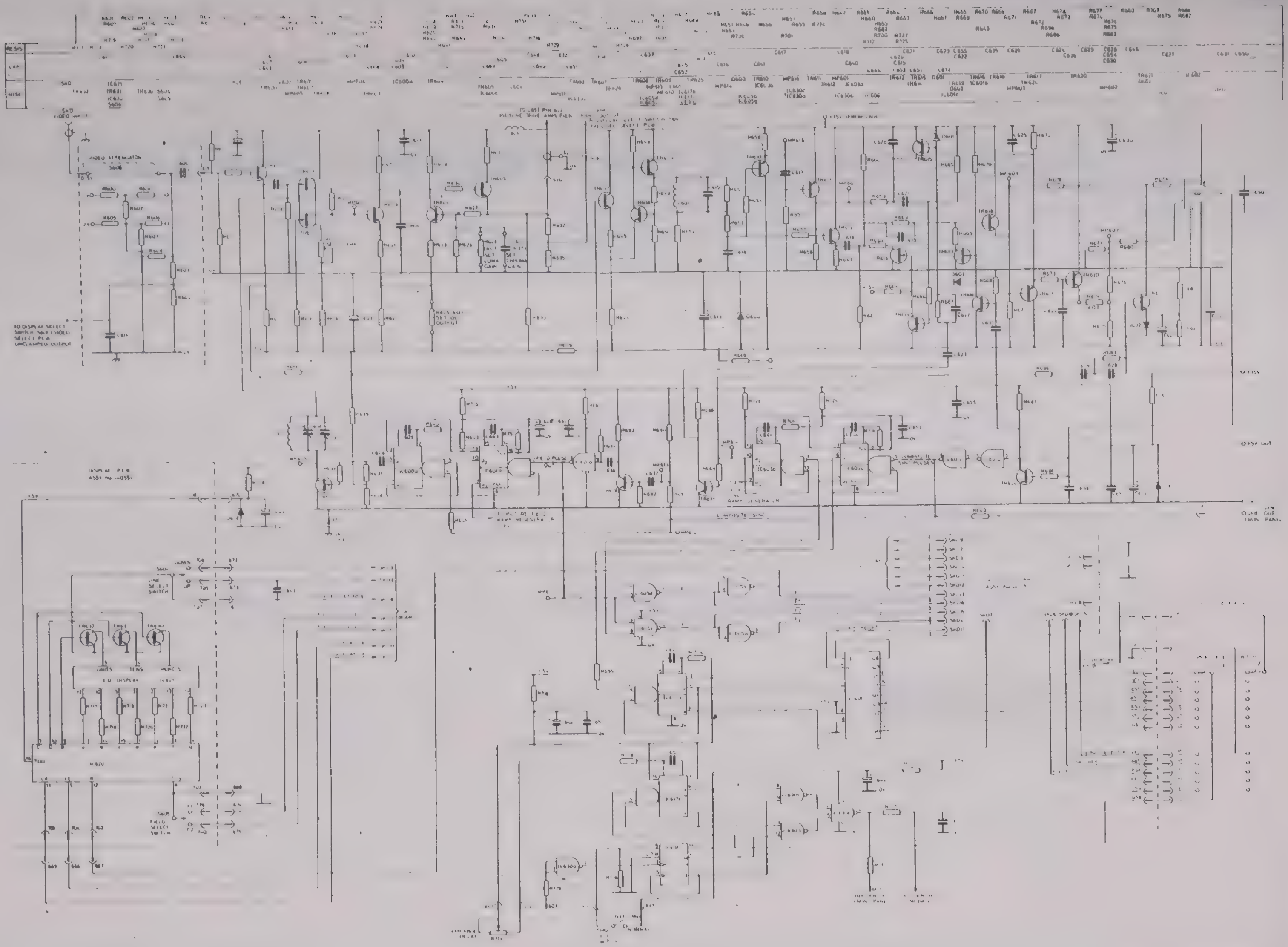


Fig. 6A Circuit Diagram T.V. Sync.

33350/5 T.V. SYNC (Cont.)

ef	Value	Description		Tol % ±	Part No
ESISTORS (Cont.)					
R717	470	CF		¼W	21797
R718	470	CF		¼W	21797
R719	470	CF		¼W	21797
R720	470	CF		¼W	21797
R721	470	CF		¼W	21797
R722	470	CF		¼W	21797
R723	470	CF		¼W	21797
R724	10	CF		¼W	21793
R725	6k8	CF		¼W	21807
R726	10k	CF		¼W	21809
R727					
R728	12k	CF		¼W	21810
R729	10k	CF		¼W	21809
R730	160k	MF	2		38647
R731	15k	MF	2		38622
R732	1k2	CF		¼W	21800
R733	680	MF	2		38590
R734					
R735	6k2	MF	2		38613
R736	820	CF	5	¼W	28724
R737	10	CF		¼W	21793
R738	4k7	CF		¼W	21805
R739	20k	MF	2		38625
R740					
R741	680	CF		¼W	28723
R742	5k6	WW			40720
R743	6k8	WW			40721
R744	100	CF		¼W	21794
R745	1k5	CF		¼W	21801
R746	3k9	CF		¼W	21804
R747	1k6	MF	2		38599
R748	47k	CF		¼W	21815
R749	4k7	CF		¼W	21805
R750	10k	CF		¼W	21809
R751	30k	MF	2		38629
R752	10M	CF	10	¼W	32661
R753	75k	MF	2		38639
R754	10M	CF	10	¼W	32661
R755	100k	CF		¼W	21819
R756	5k6	CF		¼W	21806
R757	330	CF		¼W	28721
R758	75k	MF	2		38639
R759	68k	CF		¼W	21816
R760	220k	CF		¼W	21823
R761	5k6	CF		¼W	21806
R762	36k	MF	2		38631
R763	18k	MF	2		38624
R764	15k	MF	2		38622
R765	5k6	CF		¼W	21806
R766	100k	CF		¼W	21819
R767	2k7	CF		¼W	28726
R768					
R769	33k	CF		¼W	21814
R770	2k7	CF		¼W	28726
R771	27k	MF	2		38628
R772					
R773	470	CF		¼W	21797
R776	4k3	CF	2	¼W	38609
R777	750	MF	0.5		40528
R778	250	MF	0.5		40529
R779	2k	MF	2		38601
R780	2k	MF	2		38601
R781	1k	CP			40495
R782	1k5	MF	2		38598
R783	8k2	MF	2		38616
R784	10k	MF	2		38618
R785	470	CF		¼W	21797
R786	1k	CP			40495
R787	4k7	MF	2		38610
R788	10	CF		¼W	21793
R789	47	CF		¼W	28714
R790	200k	MF	2		38649
R791	150k	MF	2		38646
R792	47k	MF	2		38634
R793	1M	MF	2		40493
R794	13k	MF	2		38621
R795	2k	CF		¼W	38601
R796	5k6	MF	2		38612
R797	2k2	CF		¼W	21802
R798	3k6	MF	2		38607
CAPACITORS					
C600	220µF	E		10V	32169
C601	22µF	T		35V	35932
C602	0.1µF	CE(1)			40466
C603	22µF	T		35V	35932
C604	.047µF	CE(2)		25V	2793
C605	5.6pF	CE(2)			22361
C606	45pF	TRIMMER			36274
C607	560pF	PS			37686
C608	0.27µF	CE(1)			40467
C609	220pF	PS			40477
C610	0.1µF	CE(3)		25V	36709
C611	39pF	PS	A.O.T.		37204
C612	22µF	T		35V	35932
C613					
C614					
C615	200pF	PS			44072
C616	100pF	PS			37206
C617	0.1µF	CE(1)			40466
C618	0.1µF	CE(1)			40466
C619	0.1µF	CE(1)			40466
C620					
C621	150pF	PS			40476
C622	1000pF	CE(2)			22387
C623	.047µF	CE(2)		25V	2793
C624	0.1µF	CE(1)			40466
C625	0.27µF	CE(1)			40467
C626	330pF	PS			40479
C627	22µF	T		35V	35932
C628	1000pF	CE(2)			22387

OS3350/5 T.V. SYNC (Cont.)

CAPACITORS (Cont.)

Ref	Value	Description	Tol %±		Part No
C629	.047µF	CE(2)		25V	2793
C630	1µF	T		35V	34895
C631	1µF	T		35V	34895
C632	.047µF	CE(2)		25V	2793
C635	270pF	PS			40478
C636	100pF	PS			37206
C637	3600pF	PS	2½	63V	40484
C638	5600pF	PS	2½	63V	40486
C639					
C640	4700pF	PS	2½	63V	40485
C641	680pF	PS			40481
C642					
C643	100pF	CE(2)			22376
C644	33µF	E		16V	32173
C645	430pF	PS			40480
C646	22µF	T		35V	35932
C647	33µF	E		16V	32173
C648	33µF	T		10V	40463
C649	33µF	E		16V	32173
C650	.01µF	CE(2)		250V	22395
C651	0.1µF	CE(1)			40466
C652	5600pF	PS	2½	63V	40486
C653	.01µF	CE(2)		250V	22395
C654					
C655	0.22µF	CE(3)		6V	43290
C656	330pF	CE(2)			22381
C657	6.8µF	T		35V	37696
C658	330pF	PS			40479
C659	4.7µF	T		35V	53249
C660	22µF	T		35V	35932
C661	6.8µF	T		35V	37696
C662	22µF	T		20V	40462
C663	.01µF	CE			40465
C664	0.1µF	CE(1)			40466
C665	0.33µF	CE(3)	10	50V	40469
C666	6.8µF	T		35V	37696
C667	6.8µF	T		35V	37696
C668	6.8µF	T		35V	37696
C669	.01µF	CE(2)		250V	22395
C670	6.8µF	T		35V	37696
C671	0.1µF	CE(1)			40466
C672	150pF	CE(2)			22378
C673	.047µF	CE(2)		25V	2793
C674	6200pF	PS	2½	63V	40487
C675	1µF	T		35V	34895
C676					
C677	0.33µF	CE(2)	10	50V	40469
C678	.01µF	CE(2)		250V	22395
C679	22µF	T		35V	35932
C680	.01µF	CE(2)		250V	22395
C682	10pF	PS	2½	125V	40471
C683	8.2pF	PS	2½	125V	40470
C684	45pF	TRIMMER			36274
C685	.01µF	CE(2)		250V	22395

Ref	Value	Description	Tol %±	Part No
C686	.01µF	CE(2)	250V	22395
C687	.01µF	CE(2)	250V	22395

TRANSISTORS

Ref	Value	Description	Tol %±	Part No
TR600		MPS2369		37096
TR601		AE31	Dual f.e.t.	A36243
TR602				
TR603		MPS2369		37096
TR604		MPS2369		37096
TR605		MPS2369		37096
TR606		BF244A		36354
TR607		BC182B		33205
TR608		BC182B		33205
TR609		BC182B		33205
TR610		BCY71		40497
TR611		BCY71		40497
TR612		BC182B		33205
TR613		E112		40499
TR614		MPS2369		37096
TR615		BCY71		40497
TR616		BC182B		33205
TR617		BCY71		40497
TR618		BC182B		33205
TR619		E112		40499
TR620		BC182B		33205
TR621		BC182B		33205
TR624		BC182B		33205
TR625		MPS2369		37096
TR626		BC182B		33205
TR630		MPS2369		37096
TR631		MPS2369		37096
TR632		MPS2369		37096
TR633		BC182B		33205
TR634		BC182B		33205
TR635		MPS2369		37096
TR636		BC182B		33205
TR637		BCY70		70182
TR638		BCY70		70182
TR639		BC182B		33205
TR640		BC182B		33205
TR641		BF244		36846
TR644		BC108		26110
TR645		BC108		26110
TR646		2N3906		21533
TR647		2N930		21548
TR648		2N3906		21533

DIODES

Ref	Value	Description	Tol %±	Part No
D600	6V2	ZENER		33930
D601		IN4148		23802
D602		IN4148		23802
D603		IN4148		23802

S3350/5 T.V. SYNC (Cont.)

Ref	Value	Description	Tol % ±	Part No
DIODES (Cont.)				
D605	5V1	ZENER		33928
D606	5V1	ZENER		33928
D609		IN4148		23802
D610	24V	ZENER		33944
D612		IN4148		23802
D613		IN4148		23802
D614		IN4148		23802
D615		IN4148		23802
D616	6V5	ZENER		40722
D618		IN3595		29330
D619		IN4148		23802
D620	10V	ZENER		33935
INTEGRATED CIRCUITS				
IC601		7404		31836
IC602		TL710CP		40494
IC603		96L02		40510
IC605		4011		34953
IC606		4017		37689

Ref	Value	Description	Tol % ±	Part No
IC617		4098		40509
IC620		MM74C925N		40513
IC621		HP5082-7433		40504
IC630		4011		34953
IC631		4013		34954
MISCELLANEOUS				
L601	10µH			40491
L602	3.3µH			40490
L603	100µH			40492
L604	100µH			40492
L605	3.3µH			40490
L606	3.3µH			40490
S601				A4/40711
S602				A4/44062
S603				40700
S604				44056
S605				44057
S606				A3/40695

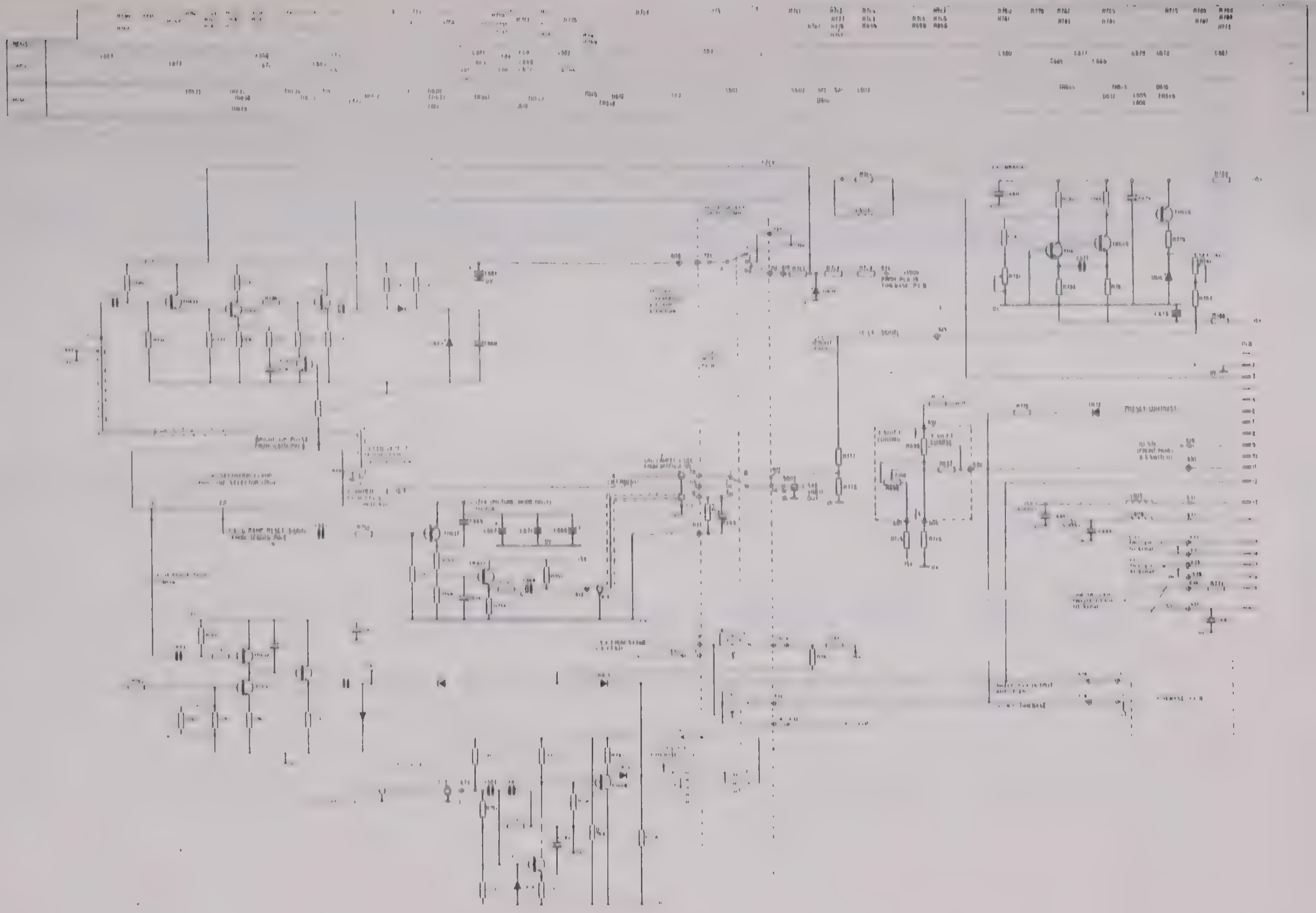


Fig. 68 Circuit Diagram T.V. Sync

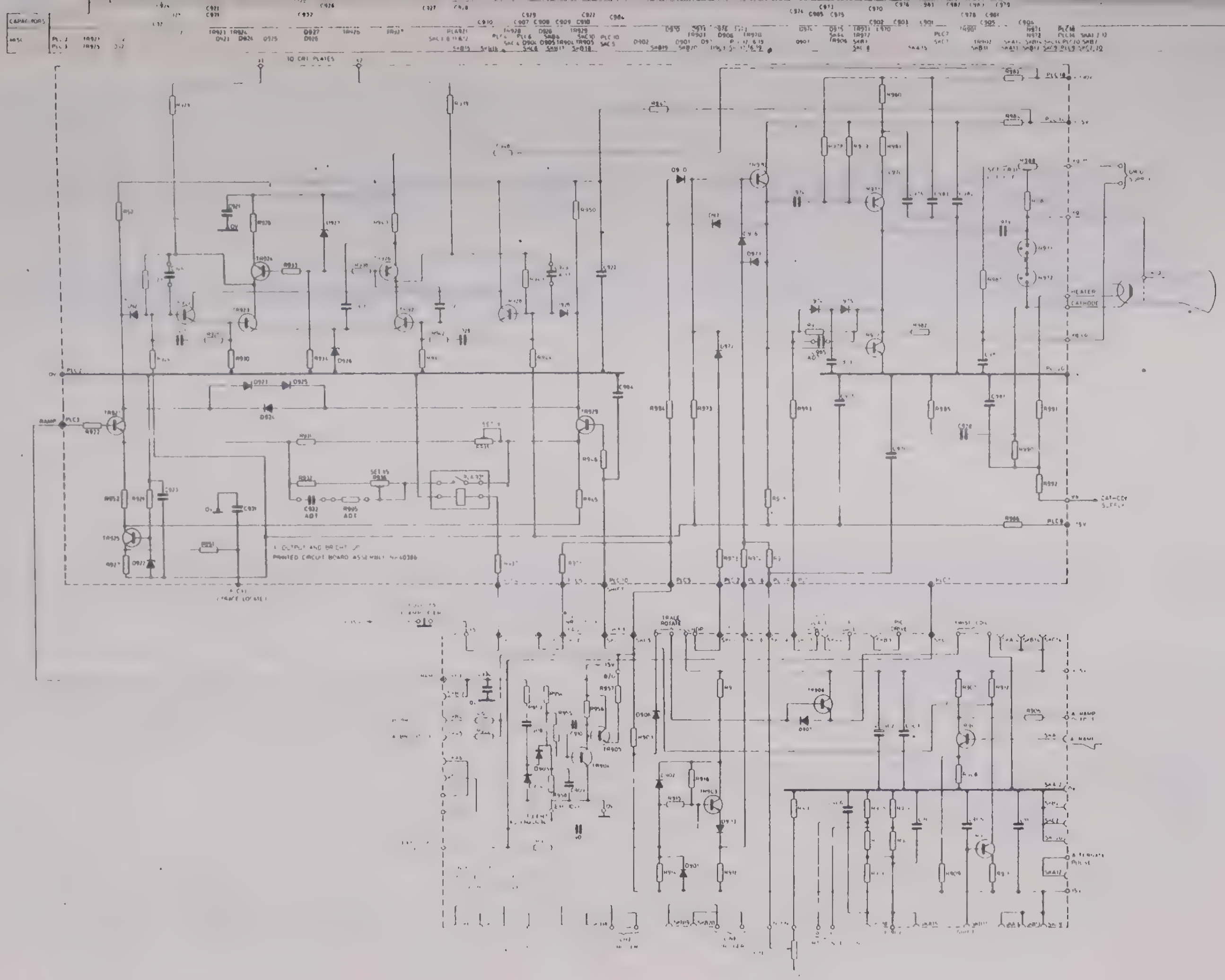
OS3350/5 'X' O/P BRIGHT UP INTERCONNECTION PCB

Ref	*Value*	*Description*	*Tol % ±*	*Part No*	*Ref*	*Value*	*Description*	*Tol % ±*	*Part No*
RESISTORS									
R900	10	CF		21793	R955	10k	CF		21809
R901	33	CF		28712	R956	180k	CF		21822
R902	33	CF		28712	R957	1k5	CF		21801
R903	47k	CF		21815	R958	1k	CF		21799
R904	68k	CF		21816					
R905	47k	CF		21815	R961	270	CF		28720
R906	330	CF		28721	R962	270	CF		28720
R907	4k7	MO		26722	R963	100	CF		21794
R908	3k9	CF		21804					
R909	Sk1	MO		28794	R970	4k7	CF		21805
R910	680	CF		28723	R971	2k4	MF	2	38603
R911	100	CF		21794	R972	47	CF		28714
R912	47k	CF		21815	R973	3k9	CF		21804
R913	22k	CF		18566	R974	5k6	CF		21806
R914	47k	CF		21815	R975	1k8	CF		29725
R915	10k	CF		21809	R976	100	CF		21794
R916	39k	CF		29	R977	39k	MF		38632
R917	100	CF		21794	R978	82k	MF		38640
R918	2k2	CF		18554	R979	3k9	CF		21804
R919	47k	CF		21815	R980	22k	MO	1W	41483
R920	68k	CF		21816	R981	10	CF		21793
R921	10k	CF		21809	R982	47k	CF		21815
R922	100	CF		21794	R983	10	CF		21793
R923	47k	MO		28814	R984	10	CF		21793
R924	47k	CF		21815	R985	470	CF		21797
R925	150	CF		28719	R986	10	CF		21793
R926	2k2	CF		21802	R987	15M	MO		40446
R927	820	MF A.O.T.	2	38592	R988	1M	CP		40443
R928	750	MF	2	38591	R989	1M	CF		31840
R929	100	CF		21794	R990	10k	CF		21809
R930	680	CF		28723	R991	100k	CF		21819
R931	3k9	CF		21804	R992	10k	CF		21809
R932	390	CF		28722	R993	68k	MF		38638
R933	470	CF		21797	R994	47	CF		28714
R934	75k	MO		28819	R995			A.O.T.	
R935	10k	CP		40444					
R936	220	CP		40445	**CAPACITORS**				
R937	560	CF		21798	C901	.01μF	CE(2)	250V	22395
R938	470	CF	.5	21797	C902	47μF	E	25V	32182
R939	100	CF		21794	C903	.01μF	CE(2)	250V	22395
R940	750	MF	2	38591	C904	.01μF	CE(2)	250V	22395
R941	330	CF		28721	C905	.1μF	PE	16V	31377
R942	150	CF		28719	C906	.01μF	CE(2)	250V	22395
R943	47k	MO	2	28814	C907	5.6pF	CE(2)		22361
R944	47k	CF		21815	C908	.1μF		100V	37018
R945	1k5	CF		21801	C909	.01μF	CE(2)	250V	22395
R946	100	CF		21794	C910	.1μF		100V	37018
R947	10	CF		21793					
R948	100	CF	6	21794	C921	.01μF	CE(2)	250V	22395
R949	10	CF		21793	C922	.01μF	CE(2)	250V	22395
R950	10k	CF		21809	C923	.01μF	CE(2)	250V	22395
R951	6k8	CF		21807	C924				
R952	1k5	CF		21801	C925	100pF	CE(2)		22376
R953	47k	CF		21815	C926	.1μF	PE	160V	31377
R954	10M	CF		32661	C927	.01μF	CE(2)		22395

S3350/5 'X' O/P BRIGHT UP INTERCONNECTION PCB (Cont.)

ef	Value	Description	Tol %±	Part No
APACITORS				
928	100pF	CE(2)	500V	22376
929			A.O.T.	
930	120pF			22377
931	.01μF	CE(2)	250V	22395
932			A.O.T.	
970	.01μF	CE(2)	250V	22395
C973	2.7pF	CE(2)		816
C974	820pF	CE(2)		22386
C975	.01μF	CE(2)	250V	22395
C976	.1μF	PE	160V	31377
C978	.01μF	CE(2)	2.5kV	40450
C979	.01μF	CE(2)	2.5kV	40450
C980	2200pF	CE(2)	500V	22389
C981	.01μF	CE(2)	2.5kV	40450
C982	.01μF	CE(2)	250V	22395
C983	.01μF	CE(2)	250V	22395
C984	.01μF	CE(2)	250V	22395
C985			A.O.T.	
TRANSISTORS				
TR901		BC107		26790
TR902		2N3906		21533
TR903		BC108		26110
TR904		BC182B		33205
TR905		BC182B		33205
TR921		BC182B		33205
TR922		BC182B		33205
TR923		MPSU04		38723
TR924		BF470		38416
TR925		2N2369		23307
TR926		BF470		38416
TR927		MPSU04		38723
TR928		BC182B		33205
TR929		BC182B		33205

Ref	Value	Description	Tol %±	Part No
TR970		2N2369		23307
TR971		BC450/BC448/MPS8599		40128
TR972		BC449		40129
DIODES				
D901		1N4148		23802
D902		1N4148		23802
D903		1N4148		23802
D904		1N4148		23802
D905		1N4148		23802
D921		1N4148		23802
D922	4V7	ZENER		33927
D923		1N4148		23802
D924		1N4148		23802
D925		1N4148		23802
D926	3V3	ZENER		33923
D927	6V8	ZENER		33931
D928		1N4148		23802
D970		1N4148		23802
D971		1N4148		23802
D972		1N4148		23802
D973		1N4148		23802
D974		1N4149		1949
D975		1N4149		1949
D976		1N4148		23802
MISCELLANEOUS				
RL921				35357
L970		Ferrite FX1242		26986
N971				26845
N972				26845
SKA				31240
SJB				31241
SKC				31241


CAPACITORS
10 CRT PLATES
0V
PLC1
RAMP
PLC3
TR925
TR926
TR923
TR929
R952
C931
C932
ADT
R935
ADT
D923
D924
D925
1 OUTPUT AND BRIGHT UP
PRINTED CIRCUIT BOARD ASSEMBLY
HEATER
CATHODE
CRT-CCT
PLC8
+5V
TRACE ROTATE

2 PLC CONNECTS DIRECT TO SAC

3 —◆— INDICATES PCB EDGE CONNECTIONS

Fig. 7 Circuit Diagram 'X' Output, Bright-up & Interconnection

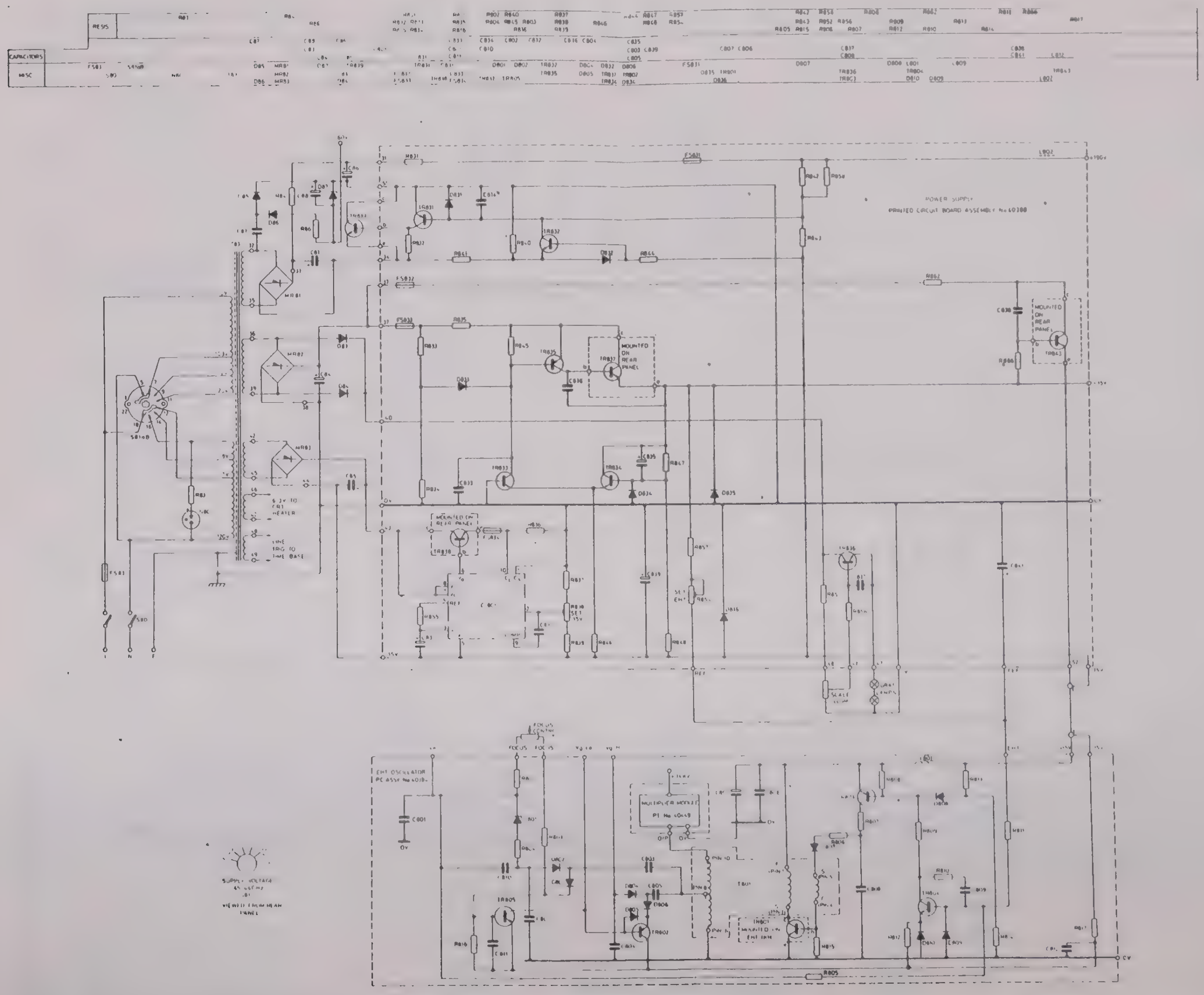
OS3350/5 POWER SUPPLY & EHT OSCILLATOR

Ref	*Value*	*Description*	*Tol %±*	*Part No*
RESISTORS				
R83	68k	CF		21816
R84	47	WW	5	18739
R85				
R86	4k7	CF		21805
R802	1M2	MG		33589
R803	2M7	MG		40448
R804	10k	CF		21809
R805	15M	MG		40446
R806	220	CF		21796
R807	1k5	CF		21801
R808	5k6	CF		21806
R809	3k3	CF		21803
R810	1k	CF		21799
R811	68k	CF		21816
R812	6k8	CF		21807
R813	120	CF		28718
R814	1k3	MF	2	38597
R815	1k	CF		21799
R816	2k2	CF		21802
R817	10	CF		21793
R831	22	CF	2½W	42710
R832	470	CF		21797
R833	180	CF		21795
R834	3k3	CF		21803
R835	0R82	WW	2½W	31889
R836	0R82	WW	2½W	31889
R837	7k5	MO	2	28797
R838	1k	PCP		26870
R839	6k8	MO	2	28796
R840	820	CF		28724
R841	2k7	CF	1W	19043
R842	100k	MO	2	28822
R843	3k6	MO	2	26725
R844	4k7	CF		21805
R845	1k	CF		21799
R846	4k7	CF		21805
R847	7k5	MO	2	28797
R848	7k5	MO	2	28797
R852	470	CF		21797
R853				
R854	47k	PCP		28335
R855	3k3	CF		21803
R856	100	CF		21794
R857	22k	CF		21812
R858	91	MO	2	28821
R862	1	WW	3W	31890
R866	47	WW		18739
CAPACITORS				
C83	100µF + 200µF	E	275V	24740
C84	4700µF	E	40V	43532
C85	4700µF	E	40V	43532
C86	100µF + 200µF	E	275V	24740
C87	.22µF	PE	400V	31396
C88	4.7µF	PE	63V	32195
C801	4700pF		4kV	26863
C802	4700pF		4kV	26863
C803	4700pF		4kV	26863
C804	500pF		8kV	26862
C805	500pF		8kV	26862
C806	0.1µF		25V	36709
C807	68µF	T	25V	54337
C808	.33µF	PE	160V	35603
C809	150pF	CE(2)	500V	22378
C810	.01µF	CE(2)	250V	22395
C811	100µF	T	6V3	35714
C812	2.2µF		30V	35930
C831	10µF	E	25V	32180
C832	100pF	CE(2)	500V	22376
C833	.01µF	CE(2)	250V	22395
C834	3000pF	CE(2)	500V	22391
C835	10µF	E	25V	32180
C836	.01µF	CE(2)	250V	22395
C837	.01µF	CE(2)	250V	22395
C838	.01µF	CE(2)	250V	22395
C839	22µF	E	25V	32181
C840				
C841	10µF	E	25V	32180
TRANSISTORS				
TR801		2SC1173		36188
TR802		BC212		29327
TR803		BC212		29327
TR804		BC182B		33205
TR805		2N5831		20388
TR831		BC212K		29327
TR832		BSX20		23307
TR833		BC108		26110
TR834		BC108		26110
TR835		MM1614		19320
TR836		2N3053		4039
TR837		MJE520		24739
TR838		MJE520		24739
TR839		2N5296		28630
TR843		MJE520		24739
DIODES				
D83		1N4003		32771
D84		1N4003		32771
D85		1N4007		52337
D86		1N4007		52337

DS3550/5 POWER SUPPLY & EHT OSCILLATOR (Cont.)

Ref	Value	Description	Tol %±	Part No
DIODES (Cont.)				
D87	56V	ZENER		35760
D801	120V	ZENER		40633
D802		BY409		42356
D803		BY409		42356
D804		BY409		42356
D805		1N4148		23802
D806		BY409		42356
D807		1N4148		23802
D808		1N4148		23802
D809		1N4148		23802
D810		1N4148		23802
D831		1N4148		23802
D832		1N4148		23802
D833		1N4148		23802
D834		1N4148		23802
D835		1N4003		23462
D836		1N4003		23462
MISCELLANEOUS				
IC801		μA723C		31228
L801	150μH			35826

Ref	Value	Description	Tol %±	Part No
L802		Ferrite FX1242		26986
T83				A1 40058
T801				A2 40095
N80				26586
FS83		For 110V 1A Slo-Blo		34790
FS83		For 240V 0.5A Slo-Blo		33685
FS831		250mA		32338
FS832		500mA		32339
FS833		1A		52162
FS834		1A		52162
S80			With R60	A4/31224
S81				35242
MR81		W04		29367
MR82		1N4003	4 off per	32771
MR83		W02		19725


CAPACITORS
RESIS
MISC
POWER SUPPLY
PRINTED CIRCUIT BOARD ASSEMBLY
MOUNTED ON REAR PANEL
MOUNTED ON REAR PANEL
MOUNTED ON REAR PANEL
+190V
+15V
0V
FS831
FS832
FS833
FS801
L802
MR801
MR802
MR803
TR831
TR832
TR833
TR834
TR835
TR836
TR837
TR838
TR843
D831
D832
D833
D834
D835
D836
C833
C835
C836
C838
C839
R833
R834
R835
R840
R842
R843
R844
R845
R847
R850
R852
R860
SB10B
S80
6.3V TO CRT HEATER
LINE TRIG TO TIME BASE
SET EHT
SET 15V
SCALE LAMPS
FOCUS
FOCUS
FOCUS CONTROL
EHT OSCILLATOR PC ASSY
MULTIPLIER MODULE
TB801
TR802
TR805
TR801 MOUNTED ON EHT TANK
C801
C811
R805
R815
R816
SUPPLY VOLTAGE
VIEWED FROM REAR PANEL

NOTES

1 - ● INDICATES PCB EDGE CONNECTIONS

2 - ○ INDICATES PCB CONNECTION PINS

Fig. 8 Circuit Diagram Power Supply & E.H.T. Oscillator

OS3550/5 INTERCONNECTIONS

Ref	Value	Description	Tol %±	Part No
RESISTORS				
R26	250	CP	With S12	A4/31257
R27	250	CP	With R37	A4/40453
R28	39	CF	¼W	28713
R29	39	CF	¼W	28713
R30	39	CF	¼W	28713
R31	39	CF	¼W	28713
R32	180	CF	¼W	21795
R33	180	CF	¼W	21795
R34	1M	CF	¼W	31840
R37	250	CP	With R27	
R60	4k7	CP	Part of S80	A4/31222
R80	470k	CP		A4/31222
R81	100k	CP		A4/35941
R82	4k7	CP		A4/31223
R85	8k2	WW		19802
R561		Resistor Module		A3/36454
R562				
R563				
R564				
R565				
R566				
R567				
R568				
R569				
R570				
R575	1k	CF	¼W	21799
CAPACITORS				
C23	1.5pF	SM		813
C24	27pF	CE(2)		22369
C456	68pF	SM		34353

Ref	Value	Description	Tol %±	Part No
C457	1μF	CE(2)	1 160V	24888
C458	0.1μF	CE(2)	1 160V	24887
C459	0.01μF	CE(2)	1 160V	24886
C460	900pF	CE(2)	1 125V	24885
C461	100pF	CE(2)	500V	22376
DIODES				
D441		LED		35202
MISCELLANEOUS				
V83		Thorn D14 – 310GH		40658
L83		Trace Rotation Coil		A3/35997
LP1	12V			36634
LP2	12V			36634
S12		Switch CH1 X5 With R26		A4/31257
S31		Switch 'Y' Function		40455
S43		Switch Timebase		31280
S51		Switch Trace Locate		35502
S74		Switch Time/Cm Calibrated		31280
S76		Switch X5 Magnifier With R698/699		35294
S201		Switch CH2 Invert		4069
S606		Switch Video Attenuator		A3/40695
SKA				24159
SKB				24159
SKC				24159
SKD				1222
SKE				1222

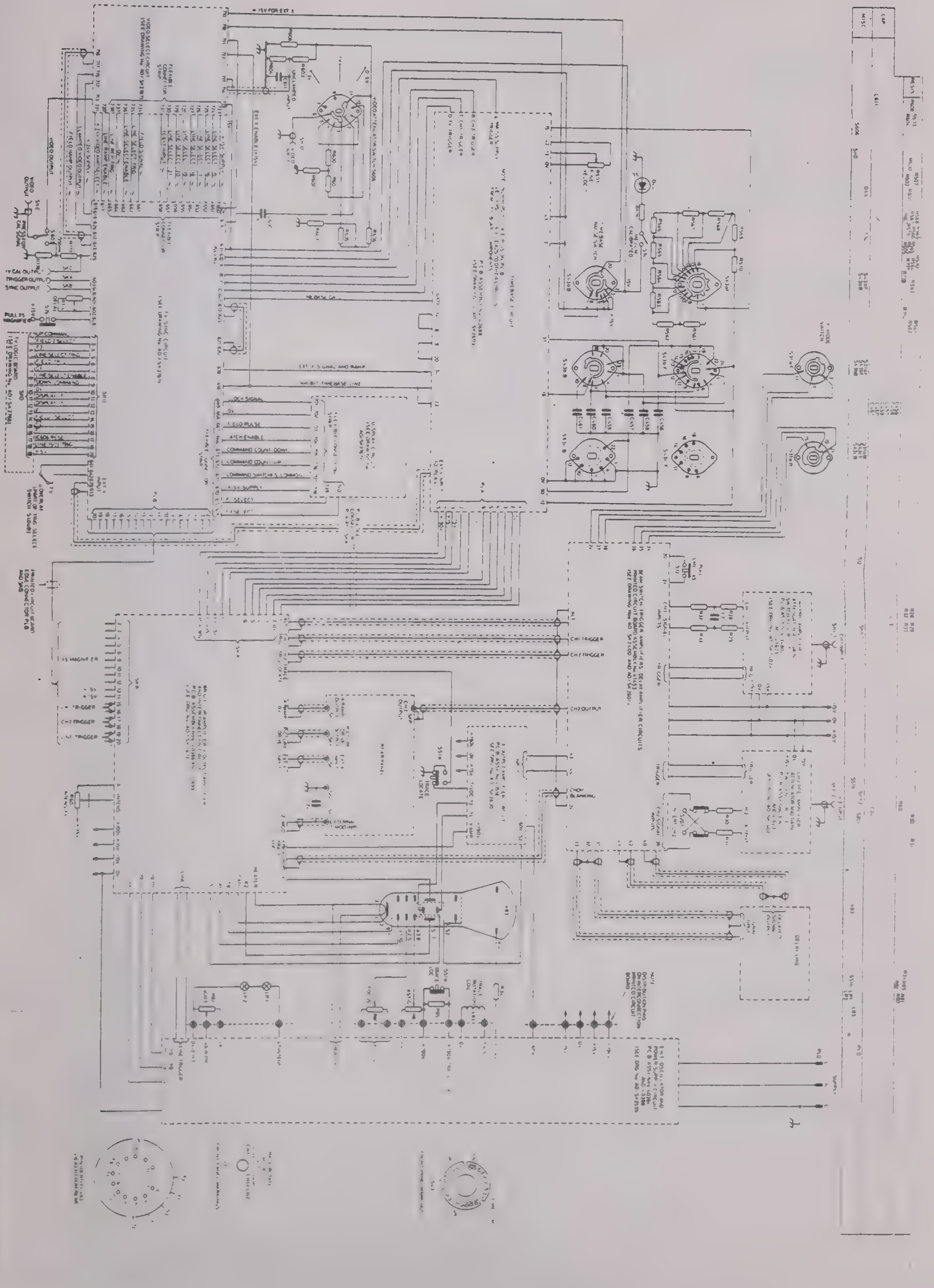

+15V FOR EXT Z
VIDEO OUTPUT
1V CAL OUTPUT
TRIGGER OUTPUT
SYNC OUTPUT
CH1 TRIGGER
CH2 TRIGGER
CH2 OUTPUT
CHOP BLANKING
DELAY LINE

Fig 9 Circuit Diagram Interconnections

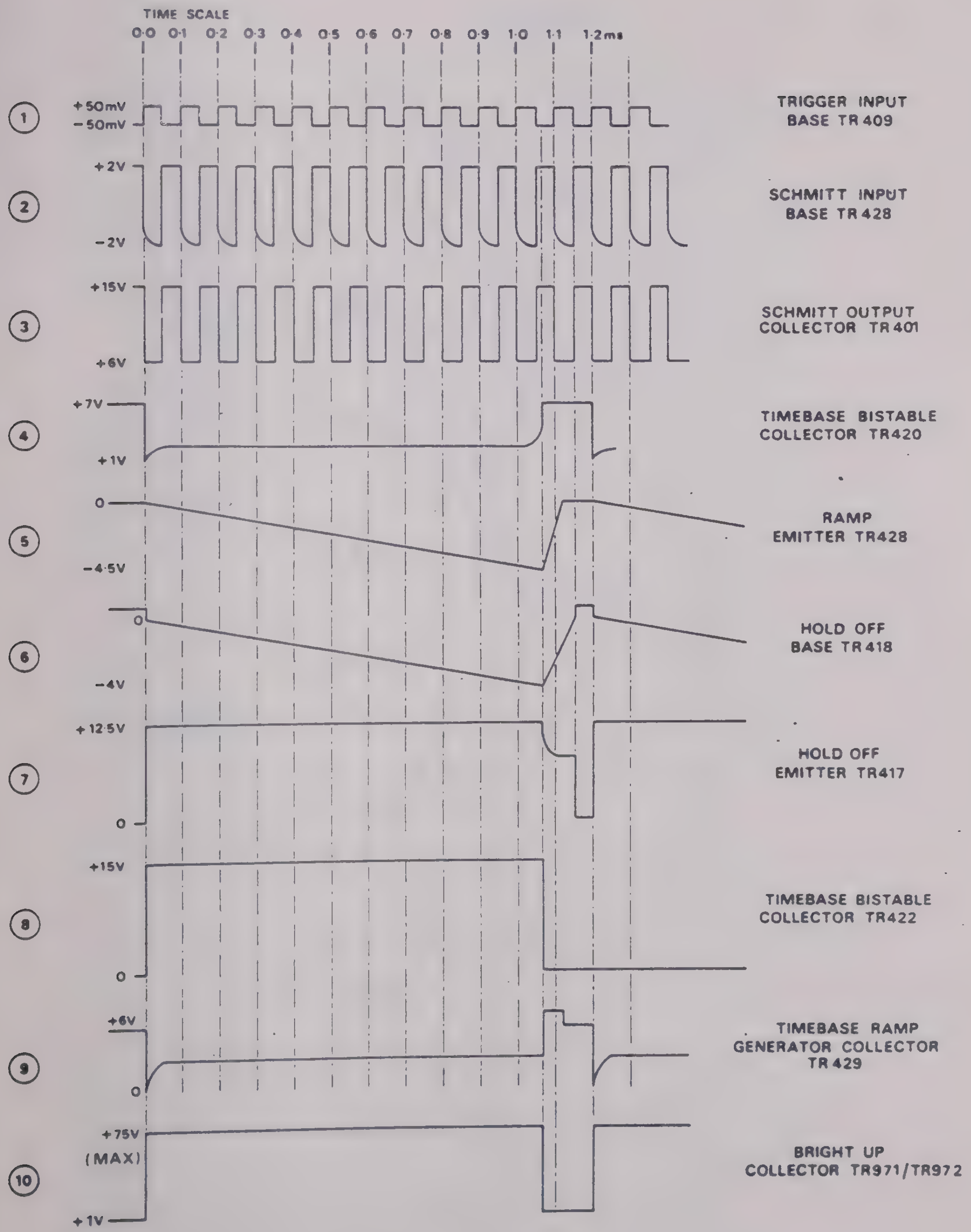

TIME SCALE
0·0 0·1 0·2 0·3 0·4 0·5 0·6 0·7 0·8 0·9 1·0 1·1 1·2ms
①
+50mV
−50mV
TRIGGER INPUT BASE TR409
②
+2V
−2V
SCHMITT INPUT BASE TR428
③
+15V
+6V
SCHMITT OUTPUT COLLECTOR TR401
④
+7V
+1V
TIMEBASE BISTABLE COLLECTOR TR420
⑤
0
−4·5V
RAMP EMITTER TR428
⑥
0
−4V
HOLD OFF BASE TR418
⑦
+12·5V
0
HOLD OFF EMITTER TR417
⑧
+15V
0
TIMEBASE BISTABLE COLLECTOR TR422
⑨
+6V
0
TIMEBASE RAMP GENERATOR COLLECTOR TR429
⑩
+75V (MAX)
+1V
BRIGHT UP COLLECTOR TR971/TR972

Fig. 10 Waveform Diagram Normal Sweep

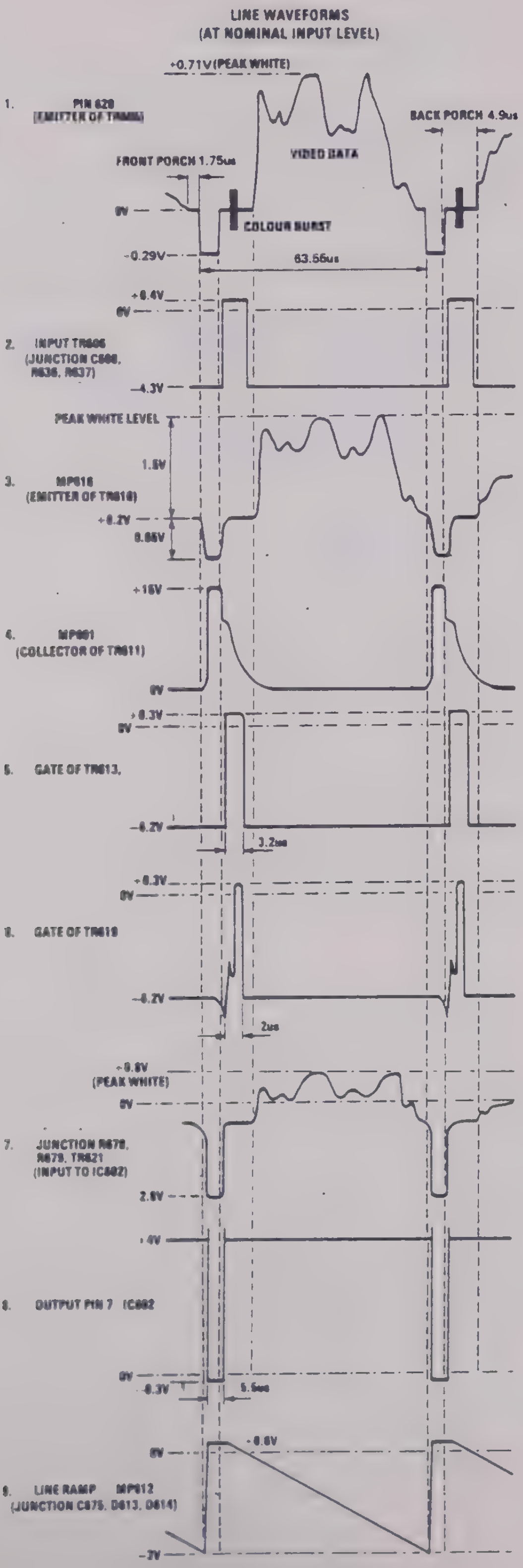

LINE WAVEFORMS
(AT NOMINAL INPUT LEVEL)
+0.71V (PEAK WHITE)
1. PIN 620 (EMITTER OF TR606)
BACK PORCH 4.9us
FRONT PORCH 1.75us
VIDEO DATA
0V
COLOUR BURST
-0.29V
63.56us
+0.4V
0V
2. INPUT TR606 (JUNCTION C608, R636, R637)
-4.3V
PEAK WHITE LEVEL
1.5V
3. MP616 (EMITTER OF TR616)
+0.2V
0.85V
+15V
4. MP601 (COLLECTOR OF TR611)
0V
+0.3V
0V
5. GATE OF TR613.
-0.2V
3.2us
+0.3V
0V
6. GATE OF TR619
-0.2V
2us
+0.8V (PEAK WHITE)
0V
7. JUNCTION R678, R679, TR621 (INPUT TO IC602)
2.8V
+4V
8. OUTPUT PIN 7 IC602
0V
-0.3V
5.5us
+0.6V
0V
9. LINE RAMP MP612 (JUNCTION C675, D613, D614)
-3V

Fig. 11 TV Waveform

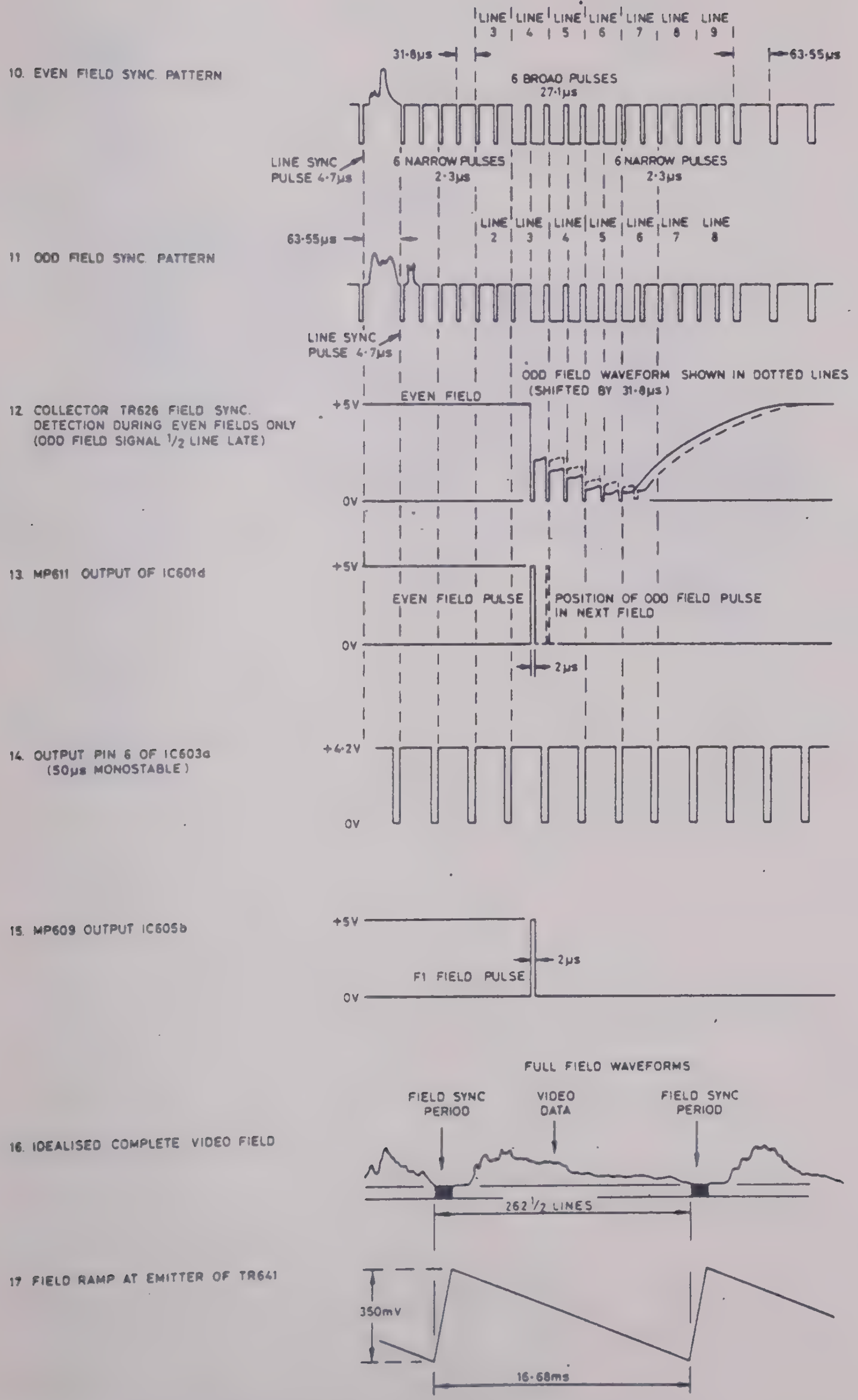

LINE 3
LINE 4
LINE 5
LINE 6
LINE 7
LINE 8
LINE 9
31·8μs
63·55μs
10. EVEN FIELD SYNC. PATTERN
6 BROAD PULSES
27·1μs
LINE SYNC PULSE 4·7μs
6 NARROW PULSES 2·3μs
6 NARROW PULSES 2·3μs
LINE 2
LINE 3
LINE 4
LINE 5
LINE 6
LINE 7
LINE 8
63·55μs
11. ODD FIELD SYNC. PATTERN
LINE SYNC PULSE 4·7μs
ODD FIELD WAVEFORM SHOWN IN DOTTED LINES (SHIFTED BY 31·8μs)
12. COLLECTOR TR626 FIELD SYNC. DETECTION DURING EVEN FIELDS ONLY (ODD FIELD SIGNAL 1/2 LINE LATE)
+5V
EVEN FIELD
0V
13. MP611 OUTPUT OF IC601d
+5V
EVEN FIELD PULSE
POSITION OF ODD FIELD PULSE IN NEXT FIELD
0V
2μs
14. OUTPUT PIN 6 OF IC603a (50μs MONOSTABLE)
+4·2V
0V
15. MP609 OUTPUT IC605b
+5V
2μs
F1 FIELD PULSE
0V
FULL FIELD WAVEFORMS
FIELD SYNC PERIOD
VIDEO DATA
FIELD SYNC PERIOD
16. IDEALISED COMPLETE VIDEO FIELD
262 1/2 LINES
17 FIELD RAMP AT EMITTER OF TR641
350mV
16·68ms

Fig. 12 Field Synch Period Waveforms

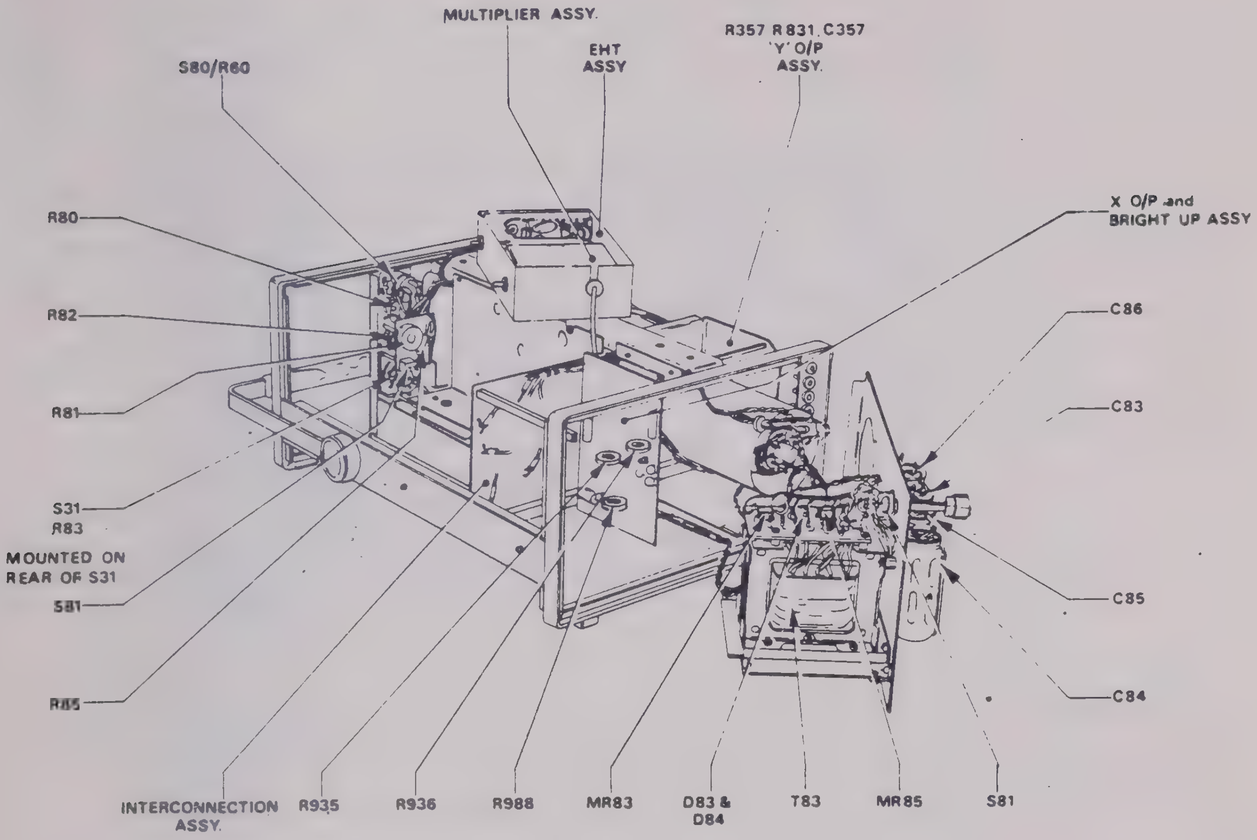

MULTIPLIER ASSY.
EHT ASSY
R357 R831 C357 'Y' O/P ASSY.
S80/R60
R80
X O/P and BRIGHT UP ASSY
R82
C86
R81
C83
S31
R83
MOUNTED ON REAR OF S31
S81
C85
R85
C84
INTERCONNECTION ASSY.
R935
R936
R988
MR83
D83 & D84
T83
MR85
S81

Fig. 13 Main Frame showing access

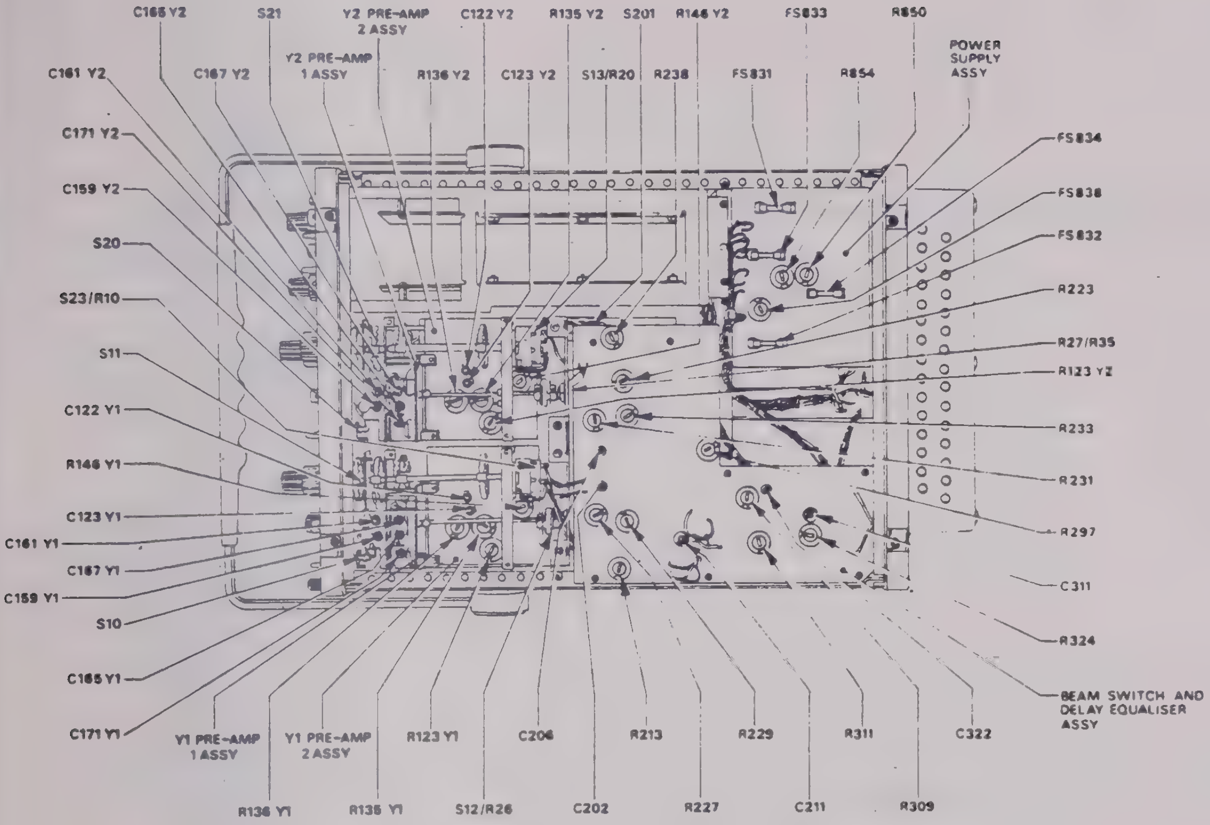

C165 Y2
S21
Y2 PRE-AMP 2 ASSY
C122 Y2
R135 Y2
S201
R146 Y2
FS833
R850
C161 Y2
C167 Y2
Y2 PRE-AMP 1 ASSY
R136 Y2
C123 Y2
S13/R20
R238
FS831
R854
POWER SUPPLY ASSY
C171 Y2
C159 Y2
S20
S23/R10
S11
C122 Y1
R146 Y1
C123 Y1
C161 Y1
C167 Y1
C159 Y1
S10
C165 Y1
C171 Y1
FS834
FS836
FS832
R223
R27/R35
R123 Y2
R233
R231
R297
C311
R324
BEAM SWITCH AND DELAY EQUALISER ASSY
Y1 PRE-AMP 1 ASSY
Y1 PRE-AMP 2 ASSY
R123 Y1
C206
R213
R229
R311
C322
R136 Y1
R135 Y1
S12/R26
C202
R227
C211
R309

Fig. 14 Underside view

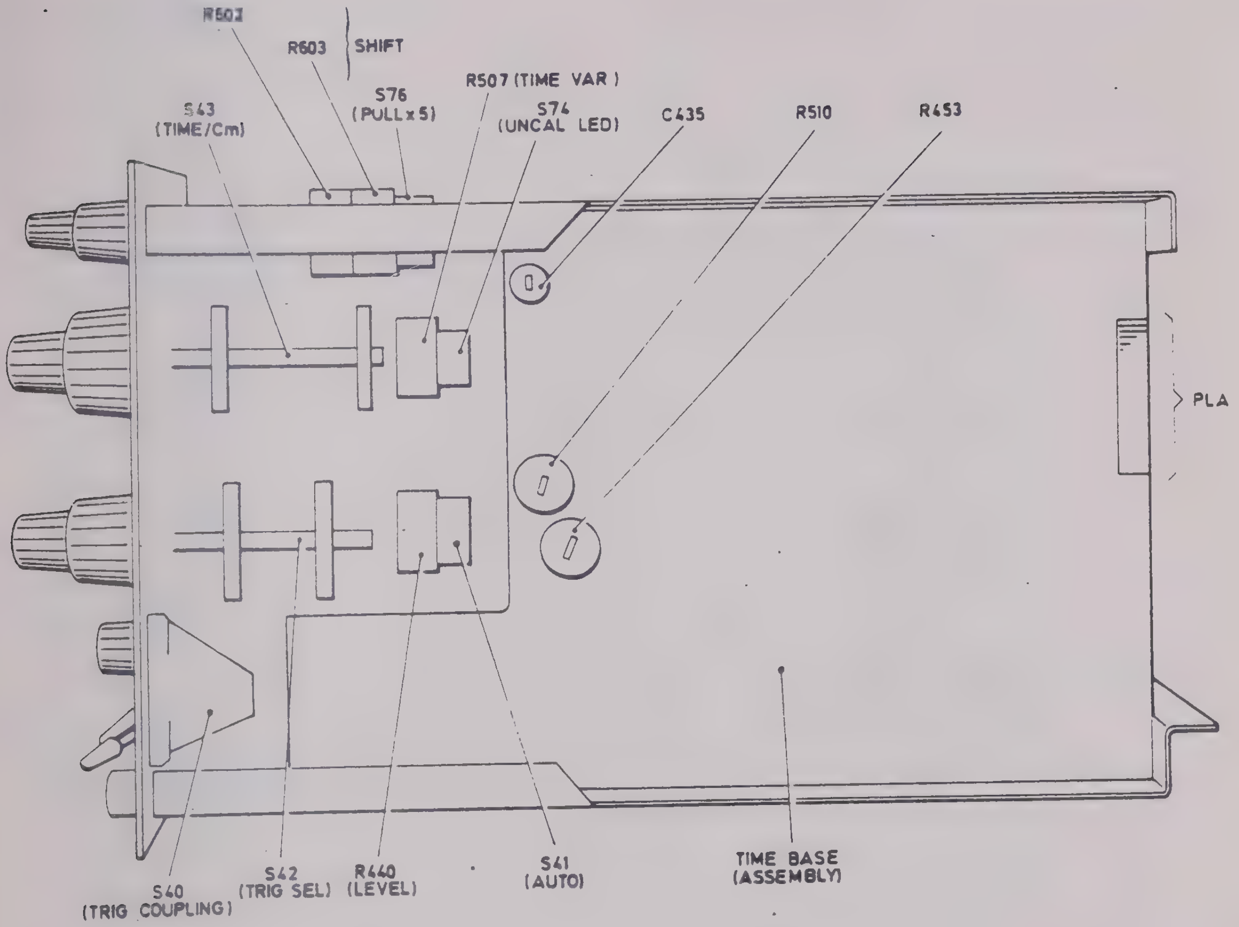

R602
R603
SHIFT
R507 (TIME VAR)
S76
(PULL x 5)
S43
(TIME/Cm)
S74
(UNCAL LED)
C435
R510
R453
PLA
S40
(TRIG COUPLING)
S42
(TRIG SEL)
R440
(LEVEL)
S41
(AUTO)
TIME BASE
(ASSEMBLY)

Fig. 15 Timebase unit right hand view

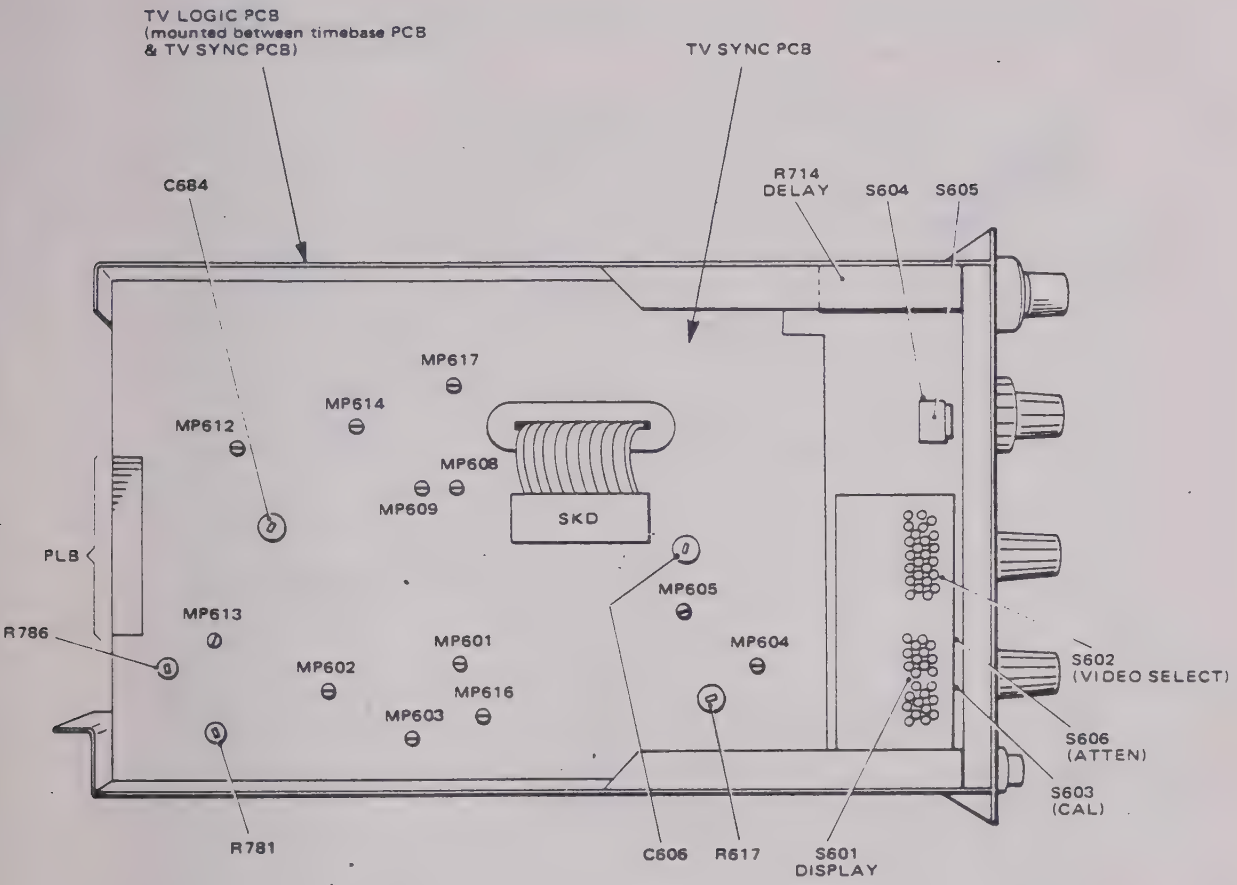

TV LOGIC PCB
(mounted between timebase PCB & TV SYNC PCB)
TV SYNC PCB
C684
R714
DELAY
S604
S605
MP617
MP614
MP612
MP608
MP609
SKD
PLB
MP605
MP613
R786
MP601
MP604
MP602
MP616
MP603
S602
(VIDEO SELECT)
S606
(ATTEN)
S603
(CAL)
R781
C606
R617
S601
DISPLAY

Fig. 16 Timebase unit left hand view

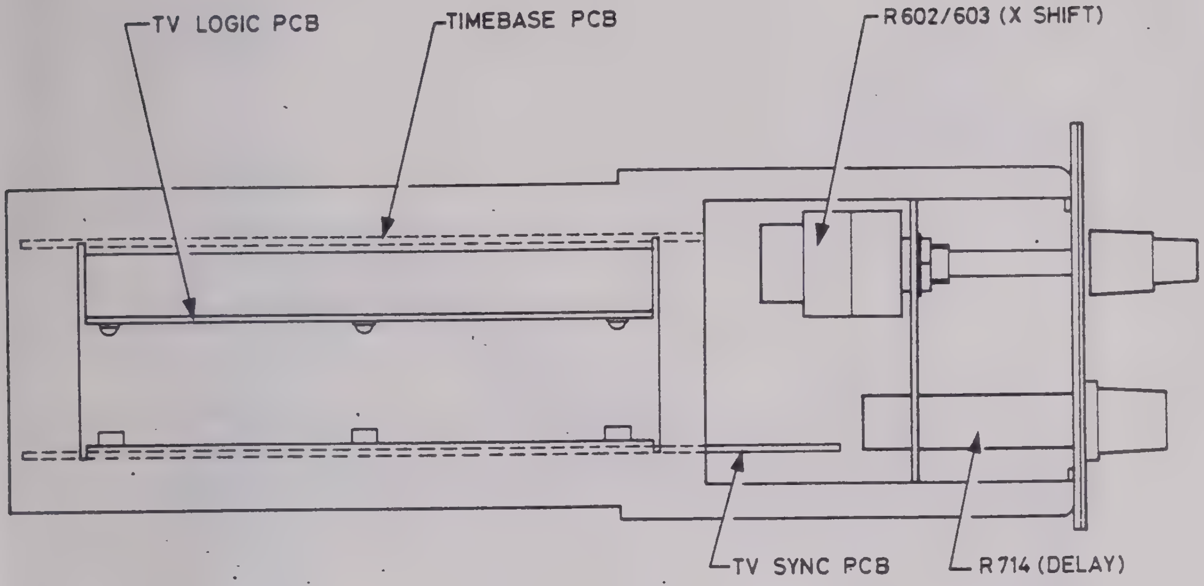

TV LOGIC PCB
TIMEBASE PCB
R602/603 (X SHIFT)
TV SYNC PCB
R714 (DELAY)

Fig. 18 Timebase Unit (Plan View)

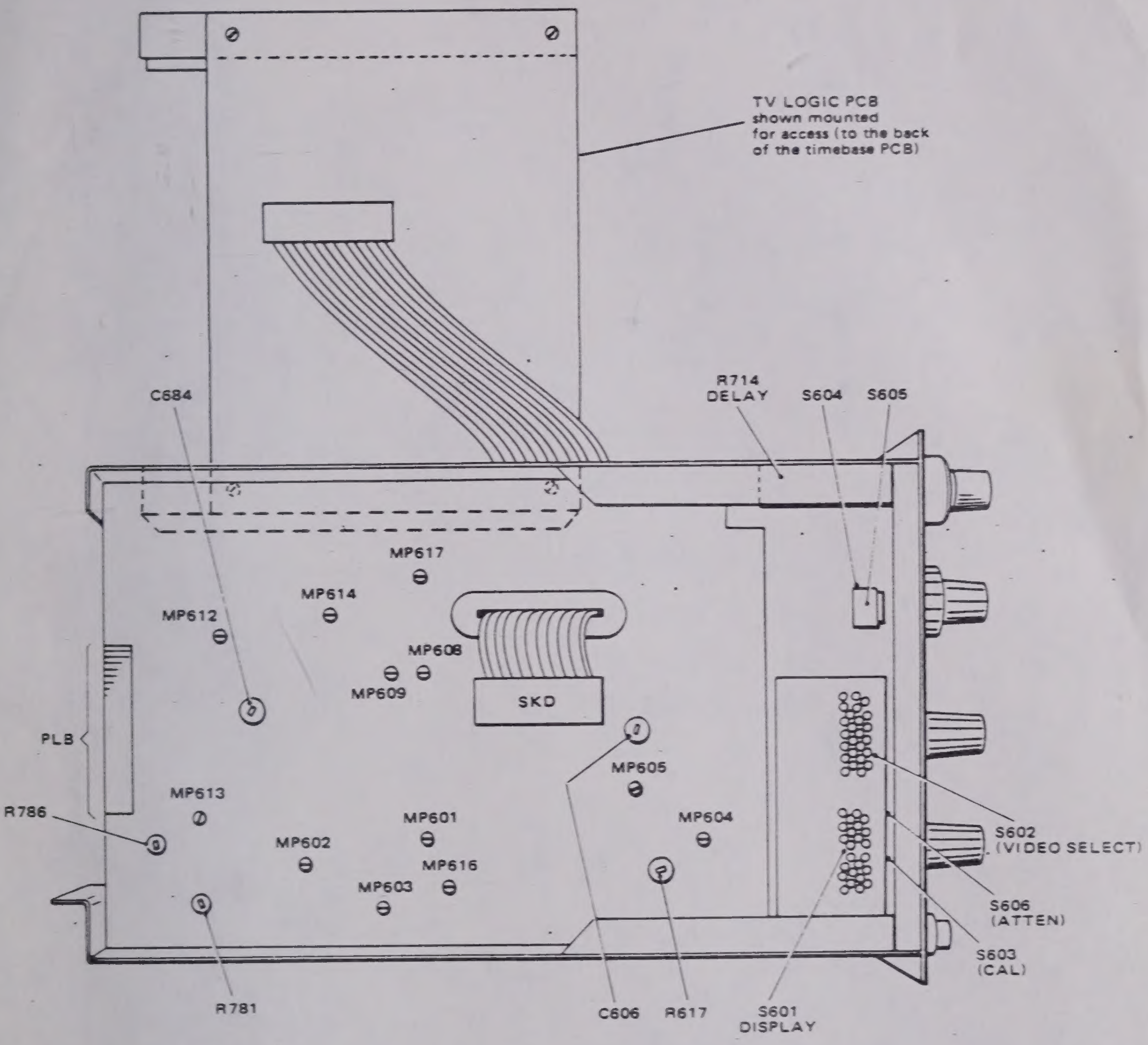

TV LOGIC PCB
shown mounted
for access (to the back
of the timebase PCB)
C684
R714
DELAY
S604
S605
MP617
MP614
MP612
MP608
MP609
SKD
PLB
MP605
MP613
R786
MP601
MP604
MP602
MP616
S602
(VIDEO SELECT)
MP603
S606
(ATTEN)
S603
(CAL)
R781
C606
R617
S601
DISPLAY

Fig. 19 Timebase Unit with T.V. Logic P.C.B. Removed

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